INTERNATIONAL STANDARD ISO/IEC 30193:2013
TECHNICAL CORRIGENDUM 1

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INTERNATIONAL ORGANIZATION FOR STANDARDIZATION • МЕЖДУНАРОДНАЯ ОРГАНИЗАЦИЯ ПО СТАНДАРТИЗАЦИИ • ORGANISATION INTERNATIONALE DE NORMALISATION
INTERNATIONAL ELECTROTECHNICAL COMMISSION • МЕЖДУНАРОДНАЯ ЭЛЕКТРОТЕХНИЧЕСКАЯ КОМИССИЯ • COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

Information technology — Digitally recorded media for information interchange and storage — 120 mm Triple Layer (100,0 Gbytes per disk) BD Rewritable disk

TECHNICAL CORRIGENDUM 1

Technologies de l'information — Supports enregistrés numériquement pour échange et stockage d'information — Disques BD réinscriptibles de 120 mm triple couche (100,0 Go par disque

RECTIFICATIF TECHNIQUE 1

Technical Corrigendum 1 to ISO/IEC 30193:2013 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 23, *Digitally Recorded Media for Information Interchange and Storage*.

Page 23, 10.7

Replace the third paragraph:

> "If the step from the top surface in the area to the top surface in the Information Area is > h_{16} = 0,2 mm, then the slope down to the top surface of the Information Area shall be smooth and l_1 < 1,8 mm as indicted in Figure 14. If the top surface in the Information Area is stepped down from the top surface in the Second transition Area, then the step shall end within diameter d_8 = 40,0 mm."

with:

> "The step from the top surface in the area to the top surface in the Information Area is h_{16}. The distance between the start and the end diameter of the step is l_1. If h_{16} > 0,2 mm, then the slope down to the top surface of the Information Area shall be smooth and l_1 shall be > 1,8 mm as indicted in Figure 14. If the top surface in the Information Area is stepped down from the top surface in the Second transition Area, then the step shall end within diameter d_8 = 40,0 mm."

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Page 24, 10.7

Replace the forth paragraph:

On Recording Layer L2
- Inner Zone 2
- Inner Zone 2
- Lead-out Zone (Outer Zone 2)

with

On Recording Layer L2
- Inner Zone 2
- Data Zone 2
- Lead-out Zone (Outer Zone 2)

Page 51, 13.13

Replace the top sentence:

Some conclusions:

All information bytes of the BIS Block are found in the first 15 rows of each Address Unit.
All parity bytes of the BIS Block are found in the last 16 rows of each Address Unit.
Each Address Field is found in the first 3 rows of each Address Unit (see Figure 34)

with

		byte number N,C from BIS Block			shift right (= mod(r,3))	filling in upward direction
			column e			
Unit *u*	row *r*	0	1	2		
8	0	1,0	1,1	1,2	0	start of Block row *N* = 1
	1	3,5	3,3	3,4	1	
	2	5,7	5,8	5,6	2	
	3	7,9	7,10	7,11	0	
	:					
	8	17,1	17,2	17,0	2	start of Block row *N* = 17
	:					
	30	61,18	61,19	61,20		
9	0	1,21	1,22	1,23		end of Block row *N* = 1
10	0	1,18	1,19	1,20		
11	0	1,15	1,16	1,17		
12	0	1,12	1,13	1,14		
13	0	1,9	1,10	1,11		
14	0	1,6	1,7	1,8		
15	0	1,3	1,4	1,5	0	↑ continuation of Block row *N* = 1
	1	3,8	3,6	3,7	1	
	2	5,10	5,11	5,9	2	
	:					
	7	15,2	15,0	15,1	1	start of Block row *N* = 15
	:					
	30	61,21	61,22	61,23	0	end of Block row *N* = 61

Figure 32 – Example of mapping (partial) of BIS bytes into last 8 Units

Some conclusions:

All information bytes of the BIS Block are found in the first 15 rows of each Address Unit.
All parity bytes of the BIS Block are found in the last 16 rows of each Address Unit.
Each Address Field is found in the first 3 rows of each Address Unit (see Figure 34)

Page 74, Figure 66

Replace the Figure:

nibble	bit 3	bit 2	bit 1	bit 0	
n_0	AS23	AS22	AS21	AS20	↑
n_1	AS19	AS18	:	:	*6 nibbles* ADIP address
:	:	:	:	:	
n_5	AS3	:	:	AS0	↓
n_6	AX11	:	:	:	↑
:	:	:	:	:	*3 nibbles* AUX data
n_8	AX3	:	:	AX0	↓

with

nibble	bit 3	bit 2	bit 1	bit 0	
n_0	AS23	AS22	AS21	AS20	↑
n_1	AS19	AS18	:	:	*6 nibbles* ADIP symbol
:	:	:	:	:	
n_5	AS3	:	:	AS0	↓
n_6	AX11	:	:	:	↑
:	:	:	:	:	*3 nibbles* AUX data
n_8	AX3	:	:	AX0	↓

Page 157 to 159,Figure 105 to 108

Replace these 4 Figures

byte position	bits	INFO 1 / PAC 1 location PAA
64	b_7 b_6	01 FF 80h
64	b_5 b_4	01 FF 84h
64	b_3 b_2	01 FF 88h
64	b_1 b_0	01 FF 8Ch
65	b_7 b_6	01 FF 90h
:	:	:
:	:	:
70	b_1 b_0	01 FF ECh
71	b_7 b_6	01 FF F0h
71	b_5 b_4	01 FF F4h
71	b_3 b_2	01 FF F8h
71	b_1 b_0	01 FF FCh

Figure 105 – Status bits and related INFO1/PAC1 address locations on Layer L0

byte position	bits	INFO 2 / PAC 2 location PAA
72	b_7 b_6	01 BA 00h
72	b_5 b_4	01 BA 04h
72	b_3 b_2	01 BA 08h
72	b_1 b_0	01 BA 0Ch
73	b_7 b_6	01 BA 10h
:	:	:
:	:	:
78	b_1 b_0	01 BA 6Ch
79	b_7 b_6	01 BA 70h
79	b_5 b_4	01 BA 74h
79	b_3 b_2	01 BA 78h
79	b_1 b_0	01 BA 7Ch

Figure 106 – Status bits and related INFO2/PAC2 address locations on Layer L0

byte position	bits	INFO 1 / PAC 1 location PAA
80	b_7 b_6	3E 00 00h
80	b_5 b_4	3E 00 04h
80	b_3 b_2	3E 00 08h
80	b_1 b_0	3E 00 0Ch
81	b_7 b_6	3E 00 10h
:	:	:
:	:	:
86	b_1 b_0	3E 00 6Ch
87	b_7 b_6	3E 00 70h
87	b_5 b_4	3E 00 74h
87	b_3 b_2	3E 00 78h
87	b_1 b_0	3E 00 7Ch

Figure 107 – Status bits and related INFO1/PAC1 address locations on Layer L1

byte position	bits	INFO 2 / PAC 2 location PAA
88	b_7 b_6	3E 45 80h
88	b_5 b_4	3E 45 84h
88	b_3 b_2	3E 45 88h
88	b_1 b_0	3E 45 8Ch
89	b_7 b_6	3E 45 90h
:	:	:
:	:	:
94	b_1 b_0	3E 45 ECh
95	b_7 b_6	3E 45 F0h
95	b_5 b_4	3E 45 F4h
95	b_3 b_2	3E 45 F8h
95	b_1 b_0	3E 45 FCh

: Figure 108 – Status bits and related INFO2/PAC2 address locations on Layer L1

with:

byte position	bits	INFO 1 / PAC 1 location PAA
64	b_7 b_6	0 01 FF 80h
64	b_5 b_4	0 01 FF 84h
64	b_3 b_2	0 01 FF 88h
64	b_1 b_0	0 01 FF 8Ch
65	b_7 b_6	0 01 FF 90h
:	:	:
:	:	:
70	b_1 b_0	0 01 FF ECh
71	b_7 b_6	0 01 FF F0h
71	b_5 b_4	0 01 FF F4h
71	b_3 b_2	0 01 FF F8h
71	b_1 b_0	0 01 FF FCh

Figure 105 – Status bits and related INFO1/PAC1 address locations on Layer L0

byte position	bits	INFO 2 / PAC 2 location PAA
72	b_7 b_6	0 01 BA 00h
72	b_5 b_4	0 01 BA 04h
72	b_3 b_2	0 01 BA 08h
72	b_1 b_0	0 01 BA 0Ch
73	b_7 b_6	0 01 BA 10h
:	:	:
:	:	:
78	b_1 b_0	0 01 BA 6Ch
79	b_7 b_6	0 01 BA 70h
79	b_5 b_4	0 01 BA 74h
79	b_3 b_2	0 01 BA 78h
79	b_1 b_0	0 01 BA 7Ch

Figure 106 – Status bits and related INFO2/PAC2 address locations on Layer L0

byte position	bits	INFO 1 / PAC 1 location PAA
80	b_7 b_6	0 7E 00 00h
80	b_5 b_4	0 7E 00 04h
80	b_3 b_2	0 7E 00 08h
80	b_1 b_0	0 7E 00 0Ch
81	b_7 b_6	07 E 00 10h
:	:	:
:	:	:
86	b_1 b_0	0 7E 00 6Ch
87	b_7 b_6	0 7E 00 70h
87	b_5 b_4	0 7E 00 74h
87	b_3 b_2	0 7E 00 78h
87	b_1 b_0	0 7E 00 7Ch

Figure 107 – Status bits and related INFO1/PAC1 address locations on Layer L1