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TECHNICAL REPORT

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Device embedding assembly technology – Part 2-9: Guidelines – Concept of JISSO Level in the electronic assembly technology industries

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FOREWORD

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IEC TR 62878-2-9 has been prepared by IEC technical committee 91: Electronics assembly technology. It is a Technical Report.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
91/1703/DTR	91/1769/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

The term and definition of JISSO Level had been developed originally at the sixth Jisso International Council (JIC) meeting held in Herndon VA, USA in May 2005 among the experts from North America, Europe and Japan on assembly/packaging technology involving semiconductors, passive devices, PWB, their materials and board design.

The term “JISSO” stands for “total solution for interconnecting, assembling, packaging, mounting and integrating system design for system integration”.

JIC started at the Headquarter of IPC in Chicago, USA in 2000 according to the agreement made by TC 91 (Electronics assembly technology, Chairman: the late Mr. Dieter Bergman) and IEC SC 47D (Semiconductor device packaging, Chairman: the late Mr. Martin G. Freedman) based on the proposal made by JNC members of TC 91 and SC 47D (Mr. Katsumi Yamamoto and Mr. Hisao Kasuga) at the 63th IEC General meeting in Kyoto in 1999.

Restructuring on JIC activities was discussed at the 14th JIC meeting held in Seoul, S. Korea in April 2013 with the following conclusion:

The purpose of this council is to provide a platform to enable a strategic collaboration among stakeholders that create benefits along the value chain of interconnecting, assembling, packaging, mounting, integrating system design, and focused technologies by increasing global awareness.

To accomplish these objectives, members will collaborate to evaluate technology and market trends, to identify and address gaps not publicly recognized, and to provide inputs or potential solutions to the electronic industry, academia, standardization bodies and regulatory institutions.

These activities will be undertaken in a spirit of responsibility to the worldwide electronic industry.

DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-9: Guidelines – Concept of JISSO Level in the electronic assembly technology industries

1 Scope

The purpose of this Technical Report is to comprise the long-term discussion among Jisso International Council (JIC) members during 1999 and 2005, when the interim agreement among all JIC members about the “concept of Jisso” as well as the “Jisso product level” for the common understanding on IEC TC 91 (electronic assembly technology) activities was reached.

Further discussion on “Jisso Product Level” could be needed among the current JIC members to finalize it in the near future based on this technical report.

2 Normative references

There are no normative references in this document.

3 Terms

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
Jisso
JISSO
total solution for interconnecting, assembling, packaging, mounting and integrating system design for system integration

4 Historical Concept of Jisso (JISSO)

4.1 Some examples of terms on Jisso/JISSO used in the past

a) Packaging

i) Total technique of interconnecting, assembling, packaging, mounting for electronic system (proposed by Prof. Rao Tummala, GIT/IBM in USA in 1991: similar to the concept of Jisso);

ii) The process of assembling one or more electronic components into a package (as per IEC 60194:2015[1] terms and definitions of IEC TC 91);

iii) The process of packing products into transportation container.

NOTE 1 Other terminologies:

– “Electronic packaging” is at least recommended when this word is being used alone.

[1] Withdrawn (cancelled and replaced by IEC 60194-1:2021 and IEC 60194-2:2017)

– “Assembling” is a common term used for various levels like electronic package (of semiconductor device), electronic module, electronic unit and electronic set

b) System integration

defined by METI and ASET(see Note 2) in 1996 in Japan

NOTE 2

METI: Ministry of Economy, Trade and Industry (Japan).

ASET: Association of Super Advanced Electronics Technologies (Japan).

c) System design and integration

proposed by Professor Nakata (Osaka University) in 1996 in Japan

d) Jisso/JISSO

Total solution for interconnecting, assembling, packaging, mounting and integrating system design for system integration as shown in Figure 1.

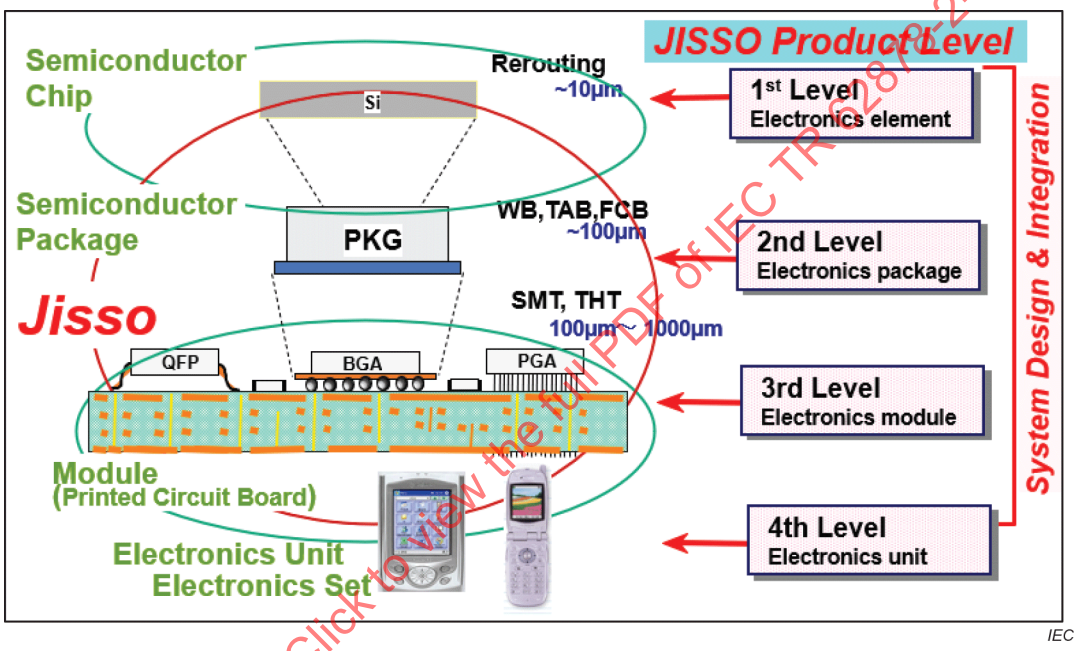


Figure 1 – Concept of Jisso/JISSO

This concept had been introduced in public by “Electronic Interconnections No. 10 – The Jisso International Council” in May 30th, 2006.

“The Jisso International Council (JIC), comprised of Asian, European and North American Jisso councils and supported by all major electronics industry trade and technology associations, including: IPC, JEITA, iNEMI, JEDEC, EIPC, JPCA and others, has just finished its 7th annual meeting. The major council co-chaired by Hisao Kasuga of NEC representing the Jisso Japan Council, Bernd Roemer of Infineon, representing the Jisso European Council and Denny Fritz of McDermid representing the Jisso North America Council. The meeting was in Berlin, Germany at IZM – Fraunhofer Institute for Reliability and Microintegration. Now, after seven years of quiet behind the scenes effort, this group of highly dedicated engineers and managers, representing electronic companies from around the world and who make up the JIC, is poised to pay some important dividends to the electronics industry.”

4.2 JISSO level versus Packaging Level (Interconnecting Level)

4.2.1 JISSO Level (typical)

The Jisso Level is proposed by Mr. Dieter Bergman, the former chairman of TC 91, IPC director as follows:

a) JISSO Level is defined by Jisso product type from a supplier to a user;

b) JISSO considers two different aspects; Functional and Physical states;

c) JISSO Product Levels are divided by Physical states;

d) JISSO Product Level is defined by Physical state before Jisso process;

e) JISSO Interface Level is defined by a type of Jisso process, such as Interconnecting process which is called “Packaging process”, or better, “Assembly process”.

NOTE The concept described in 4.2.2 created confusion when used as Packaging Levels other than “Level 1”. It became inconsistent to terminology used in general in assembly technology. In current understanding, the term “packaging” is used to describe those component manufacturing processes, which assemble functional elements into a package to form the final component. Level 2 and above cannot be called “packaging”.

4.2.2 Packaging Level

Packaging Level proposed by Professor Rao Tummala, GIT/IBM in USA in 1991 represent Interconnecting Level between the lower level and the next higher level of electronic product, such as a chip, a package, a PWB (a circuit board), Rack, board, unit, set, as shown in Figure 2.

a) “Packaging Level 1” is shown as interconnecting of chip to package like “Electronic element” (JISSO Product Level 1) to “Electronic package (JISSO Product Level 2)” using WB, TAB, FCB including Embedding technology. In other general words, “Interconnecting”, “Assembling”, “Packaging” and so on.

b) “Packaging Level 2” is shown as interconnecting of package to PWB like “Electronic package (JISSO Product Level 2)” to PWB of a circuit board of a “Electronic module (Jisso product level 3)” or a circuit board of other upper level of electronic product. In other general words, “Mounting” like SMT or THT, “Assembling”, “Soldering” and so on.

c) “Packaging Level 3” is shown as interconnecting of Rack/board to board like “Electronic module (JISSO Product Level 3) to “Electronics unit (JISSO Product Level 4)”. In another general words, “Assembling”.

Figure 2 shows the relation between a typical JISSO Level (JISSO Product Level) versus Packaging Level (Interconnecting Level).

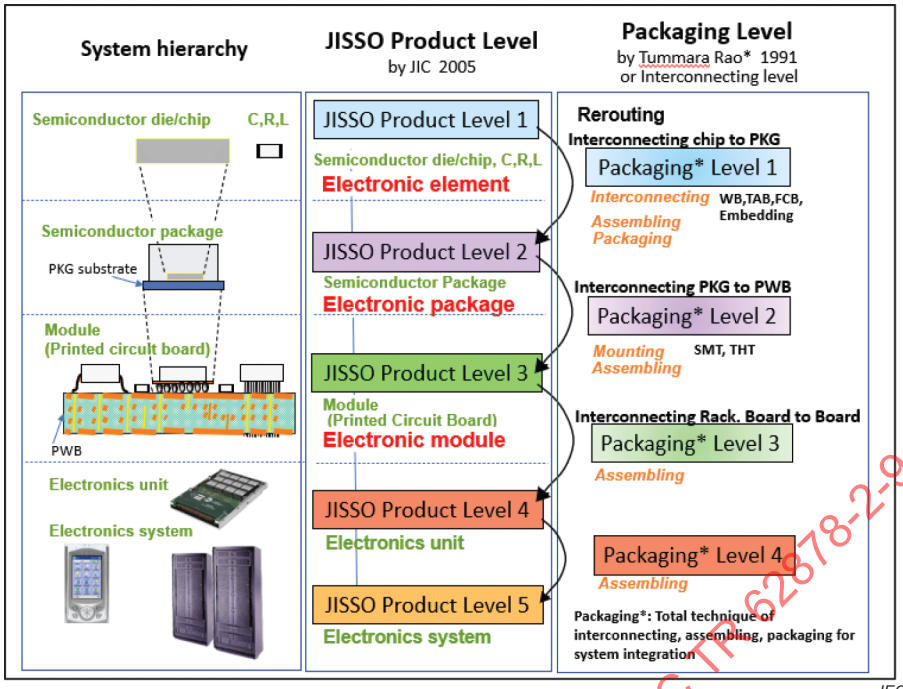


Figure 2 – Relation between JISSO Level versus Packaging Level

5 Concept of typical terms and description on JISSO Level

5.1 JISSO/Jisso

Integrated system design and manufacturing related to implementing technology solutions among user and supplier covering the technologies of interconnection, assembling, packaging, mounting and board design as shown in Figure 3 (introduced by JISSO North America Council [JNAC] in 2004) and in Figure 4 (introduced by JJC in 2005).

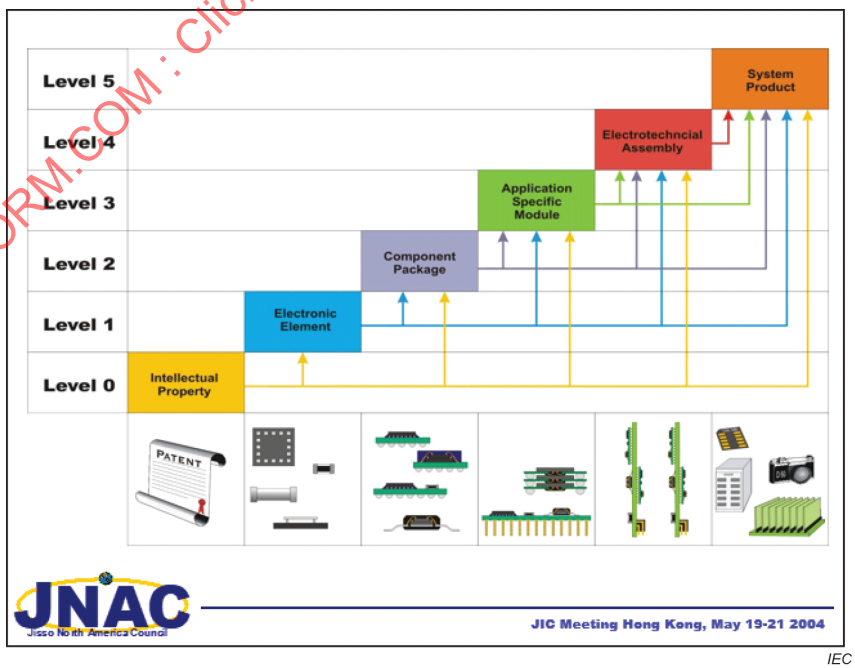
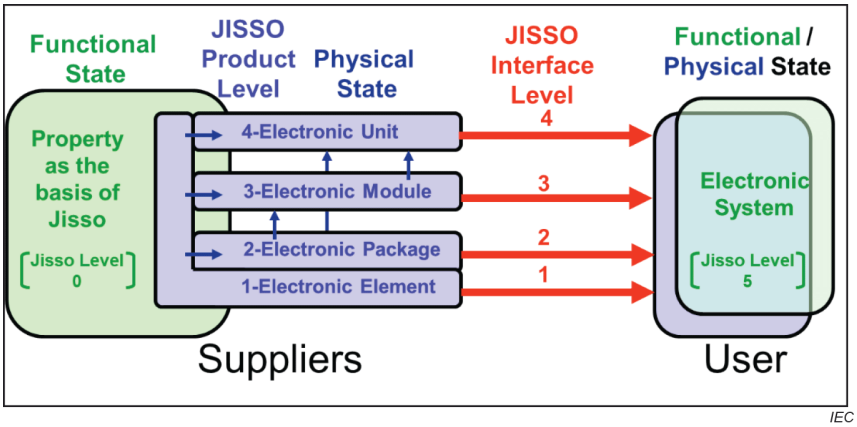


Figure 3 – JISSO Level Concept (1)
preliminarily introduced by JNAC in 2004



NOTE:

– JISSO Level is defined by Jisso type from a supplier to a user.
– JISSO considers two different aspects; Functional and Physical states.
– JISSO Levels are divided by Physical states.
– JISSO Product Level is defined by Physical state before Jisso process.
– JISSO Interface Level is defined by a type of Jisso process.

Figure 4 – JISSO Level Concept (2)

5.2 JISSO Level 0 – Intellectual information

The intellectual information and/or proprietary information of an item pertaining to the idea or intelligence imported or described in a formal document (protocol, standard, specification and/or patent disclosure) or design entity.

– The information may be in hard or soft copy and can include computer code or data format as a part of the description.
– The characteristics of the intellectual properties of an item are described as to their physical, chemical, thermal, electrical, mechanical, optical and/or environmental properties.

5.3 JISSO Product Level 1 – Electronic element

Bare die/wafer or discrete component (resistor, capacitor, inductor, transistor, diode, fuse, etc.) with metallized terminals or termination ready for mounting as shown in Figure 5.

– The element can be an IC, or discrete electrical, optical or MEMS element.
– Individual elements cannot be further reduced without destroying their stated function.

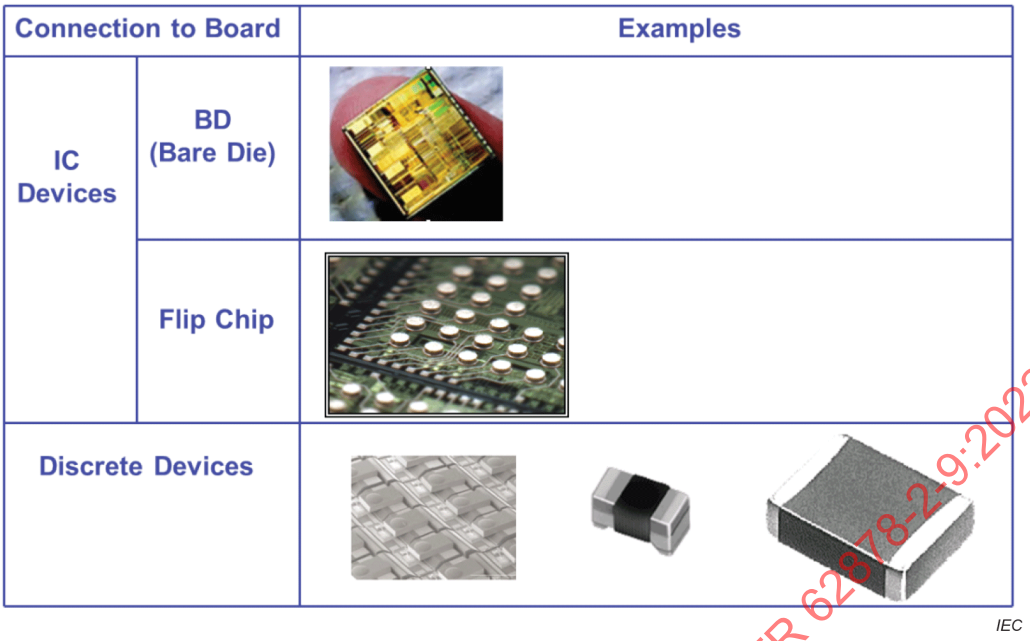


Figure 5 – Examples of JISSO Product Level 1 – Electronic element

The general concept of Level-1 terms are the following:

REMARK: Since the terms described here represent that general concept, refer to IEC 60194-2 for the formal terms authorized by IEC.

- KQD (Known Quality Die): A die-form semiconductor product for which the supplier discloses the expected defect level and potential infant mortality of the die products in the lot and the techniques used to make that determination.
- BD (Bare Die): A die-form semiconductor product for which the supplier accomplishes minimal evaluations and does not provide quality assurance information with the shipped product.
- KGD (Known Good Die): A die-form semiconductor product with quality assurance by supplier(s) equal to that of the packaged product.
- KTD (Known Tested Die): A die-form semiconductor product carried out with the probing tests equal to that of the packaged product, but without quality assurance by supplier(s).
- PD (Probed Die): A die-form semiconductor product carried out with some probing tests, but without quality assurance by supplier(s).
- Flip Chip: A leadless monolithic, circuit element structure that can be electrically and mechanically interconnected to a basic material through the use of conductive bumps.
- COB (Chip on Board): A printed board assembly technology that carries unpackaged semiconductor die(s) and interconnects them by wire bonding or similar attachment techniques. Silicon area density is usually less than that of the printed board.
- COF (Chip on Flex): A semiconductor chip mounted directly onto flexible printed board.
- SoC (System on a Chip): A nickname of an active device having complex functions.

5.4 JISSO Product Level 2 – Electronic package

An individual electronic element or elements in a container which protects the contents to assure the reliability and provides terminals to interconnect the container to an outer circuit as shown in Figure 6.

– Package outline is generally standardized or meets guideline documents.

– A Package may function as electronic, optoelectronic, or MEMS, and may in the future include Bio-electronic elements including sensors.

The general concept of Level 2 terms are the following:

REMARK: Since the terms described here represent that general concept, refer to IEC 60194-2 for the formal terms authorized by IEC.

- SCP (Single Chip Package): An Electronic Package for IC containing only one semiconductor device.
- MCP (Multi Chip Package): An Electronic Package for IC containing multiple devices.
- SMP (Surface Mount Package): An Electronic Package for Surface mount assembly type of components/devices.
- THP (Through Hole Package): An Electronic Package for Pin insertion assembly type of components/devices.
- DSP (Die Size Package): An Electronic Package the size of which is equal to the size of bare die.
- CSP (Chip Scale Package): A nickname of an Electronic Package which size is equal to the size of chip, such as FBGA (Fine pitch Ball Grid Array package), FLGA (Fine pitch Land Grid Array package) & SON (Small Outline Non-leaded package).
- SiP (System in a Package): A nickname of an electronic package having active device(s) with complex functions.

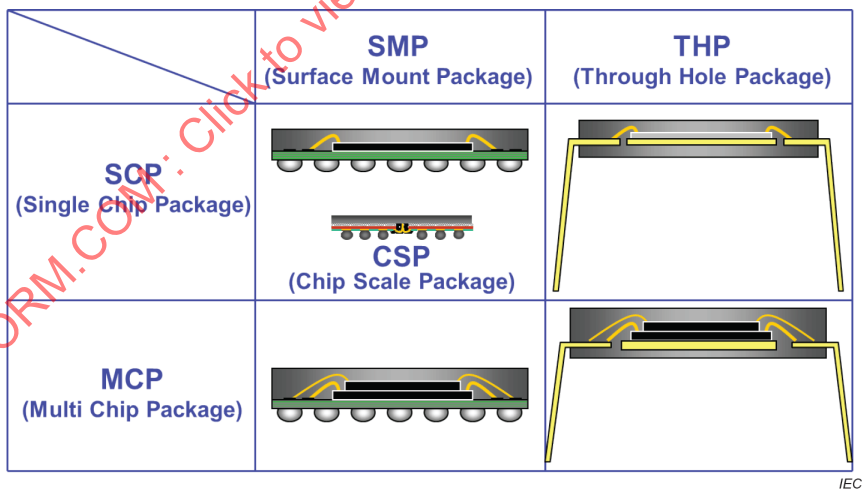


Figure 6 – Examples of JISSO Product Level 2 – Electronic package

5.5 JISSO Product Level 3 – Electronic module

A functional block which contains individual electronic elements and/or electronic packages, to be used in a next level assembly (described in 3.1 of IEC 62421:2007) as shown in Figure 7.

NOTE An individual module having an application specific function, including electronic, optoelectronic, mechanical or other elements. The module typically provides protection of its elements and packages to assure the required level of reliability.

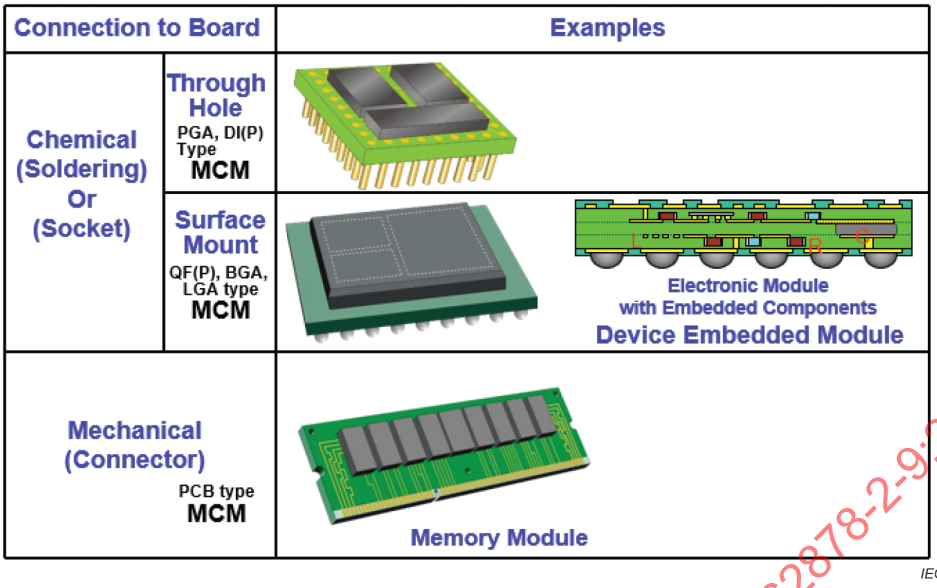


Figure 7 – Examples of JISSO Product Level 3 – Electronic module

Electronic modules may be categorized by signal interface, for example:

– wired module: a module which has only electrical interfaces (majority of present-day modules);

– wireless module: a module which has a wireless interface;

– opto-electronic module: a module which has an optoelectronic interface;

– sensor module: a module which can input physical information.

5.6 JISSO Product Level 4 – Electronic unit

A group of functional blocks that are designed to provide a single or complex function required by a system to implement the specified function as shown in Figure 8.

– The electronic unit may consist of electronic elements, electronic packages and/or electronic modules.

– The function of the electronic unit may be electronic, optoelectronic, electromechanical, or mechanical or any combination thereof.

– The function may in the future include bio- electronic applications.

Figure 8 – Example of JISSO Product Level 4 – Electronic unit

5.7 J ISSO Product Level 5 – Electronic system

A completed, market ready and dedicated product combining and interconnecting functional block(s) to perform a designated function as shown in Figure 9.

The functional block(s) mainly consist of electrotechnical assemblies and may also include electronic units, electronic modules, electronic packages and/or electronic elements.

The system product may include cabinetry or a backplane into which mounted are assemblies, modules, packages or inserted elements, and the wiring (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system.

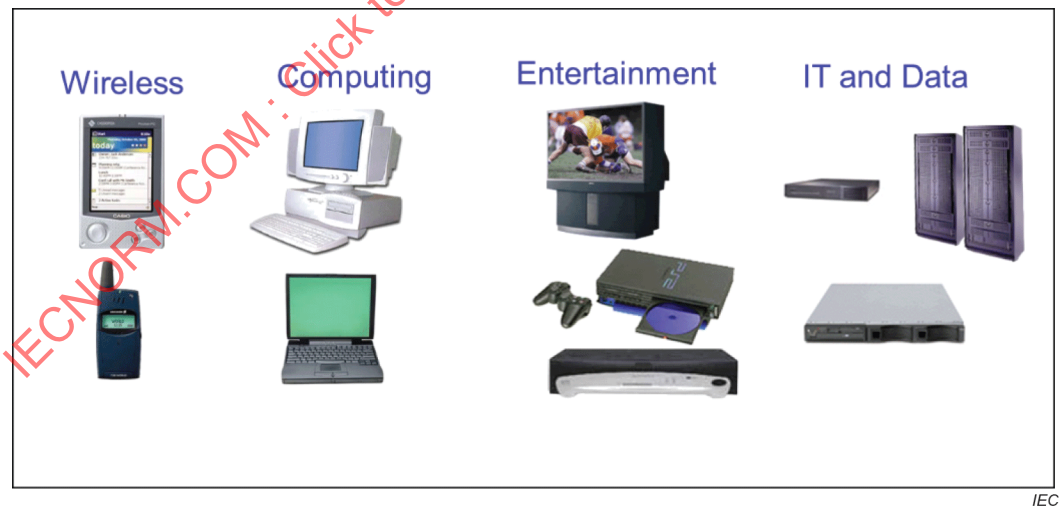


Figure 9 – Examples of JISSO product Level 5 – Electronic system