IEC 62501

Edition 2.0 2024-04
COMMENTED VERSION

INTERNATIONAL STANDARD

colour inside

Voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission – Electrical testing

IEC 62501:2024-04 CMV(en)

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 29.200, 29.240.99

ISBN 978-2-8322-8751-4

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) POWER TRANSMISSION – ELECTRICAL TESTING

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This commented version (CMV) of the official standard IEC 62501:2024 edition 2.0 allows the user to identify the changes made to the previous IEC 62501:2009+AMD1:2014 +AMD2:2017 CSV edition 1.2. Furthermore, comments from IEC SC 22F experts are provided to explain the reasons of the most relevant changes, or to clarify any part of the content.

A vertical bar appears in the margin wherever a change has been made. Additions are in green text, deletions are in strikethrough red text. Experts' comments are identified by a blue-background number. Mouse over a number to display a pop-up note with the comment.

This publication contains the CMV and the official standard. The full list of comments is available at the end of the CMV.

IEC 62501 has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment. It is an International Standard.

This second edition cancels and replaces the first edition published in 2009, Amendment 1:2014 and Amendment 2:2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) Conditions for use of evidence in lieu are inserted as a new Table 1;
b) Test parameters for valve support DC voltage test, 7.3.2, and MVU DC voltage test, 8.4.1, updated;
c) AC-DC voltage test between valve terminals, Clause 9, is restructured and alternative tests, by individual AC and DC voltage tests, added in 9.4.2;
d) Partial discharge test in routine test program is removed;
e) More information on valve component fault tolerance, Annex B, is added;
f) Valve losses determination is added as Annex C.

The text of this International Standard is based on the following documents:

Draft	Report on voting
22F/731/CDV	22F/748A/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

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VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) POWER TRANSMISSION – ELECTRICAL TESTING

1 Scope

This International Standard applies to self-commutated converter valves, for use in a three-phase bridge voltage sourced converter (VSC) for high voltage DC power transmission or as part of a back-to-back link, and to dynamic braking valves. It is restricted to electrical type and production tests.

~~The scope of this standard includes the electrical type and production tests of dynamic braking valves which may be used in some HVDC schemes for d.c. overvoltage limitation.~~

This document can be used as a guide for testing of high-voltage VSC valves used in energy storage systems (ESS). 1

The tests specified in this document are based on air insulated valves. ~~For other types of valves, The test requirements and acceptance criteria should be agreed between the purchaser and the supplier.~~ The test requirements and acceptance criteria can be used for guidance to specify the electrical type and production tests of other types of valves.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060 (all parts), *High-voltage test techniques*

IEC 60071 (all parts), *Insulation co-ordination*

IEC 60270, *High-voltage test techniques – Partial discharge measurements*

IEC 60700-1:2015, *Thyristor valves for high voltage direct current (HVDC) power transmission – Part 1: Electrical testing*
IEC 60700-1:2015/AMD1:2021

IEC 62747, *Terminology for voltage-sourced converters (VSC) for high-voltage direct current (HVDC) systems*

ISO/IEC 17025, *General requirements for the competence of testing and calibration laboratories*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62747 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1 Insulation coordination terms

3.1.1
test withstand voltage
value of a test voltage of standard waveshape at which a new valve, with unimpaired integrity, does not show any disruptive discharge and meets all other acceptance criteria specified for the particular test, when subjected to a specified number of applications or a specified duration of the test voltage, under specified conditions

3.1.2
internal insulation
air external to the components and insulating materials of the valve, but contained within the profile of the valve or multiple valve unit

3.1.3
external insulation
air between the external surface of the valve or multiple valve unit and its surroundings

3.2 Power semiconductor terms

3.2.1
turn-off semiconductor device
controllable semiconductor device which may be turned on and off by a control signal, for example an IGBT

Note 1 to entry: There are several types of turn-off semiconductor devices which can be used in VSC converters for HVDC. For convenience, the term IGBT is used throughout this standard to refer to the main turn-off semiconductor device. However, the standard is equally applicable to other types of turn-off semiconductor devices.

3.2.2
insulated gate bipolar transistor IGBT
turn-off semiconductor device with three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C)

Note 1 to entry: By applying appropriate gate to emitter voltages, the load current can be controlled, i.e. turned on and turned off.

3.2.3
free-wheeling diode
FWD
power semiconductor device with diode characteristic

Note 1 to entry: A FWD has two terminals: an anode (A) and a cathode (K). The current through FWDs is in the opposite direction to the IGBT current.

Note 2 to entry: FWDs are characterized by the capability to cope with high rates of decrease of current caused by the switching behaviour of the IGBT.

3.2.4
IGBT-diode pair
arrangement of IGBT and FWD connected in inverse parallel

3.3 Operating states of converter

3.3.1
blocking state
condition of the converter, in which a turn-off signal is applied continuously to all IGBTs of the converter

Note 1 to entry: Typically, the converter is in the blocking state condition after energization.

3.3.2
de-blocked state
condition of the converter, in which turn-on and turn-off signals are applied repetitively to IGBTs of the converter

3.3.3
valve protective blocking
means of protecting the valve or converter from excessive electrical stress by the emergency turn-off of all IGBTs in one or more valves

3.3.4
voltage step level
voltage step caused by switching of a valve or part of a valve during the de-blocked state of the converter

Note 1 to entry: For valves of the controllable voltage source type, the voltage step level corresponds to the change of voltage caused by switching one submodule or cell. For valves of the switch type, the voltage step level corresponds to the change of voltage caused by switching the complete valve.

Note 2 to entry: Annex A gives an overview of VSC converters in HVDC power transmission.

3.4 VSC construction terms

3.4.1
VSC phase unit
equipment used to connect the two DC busbars to one AC terminal

3.4.2
switch type VSC valve
arrangement of IGBT-diode pairs connected in series and arranged to be switched simultaneously as a single function unit

3.4.3
controllable voltage source type VSC valve
complete controllable voltage source assembly, which is generally connected between one AC terminal and one DC terminal

3.4.4
diode valve
semiconductor valve containing only diodes as the main semiconductor devices, which might be used in some VSC topologies

3.4.5
dynamic braking valve
complete controllable device assembly, which is used to control energy absorption in braking resistor or other components

3.4.6
valve
VSC valve, dynamic braking valve or diode valve according to the context

3.4.7
submodule
part of a VSC valve comprising controllable switches and diodes connected to a half bridge or full bridge arrangement, together with their immediate auxiliaries, storage capacitor, if any, where each controllable switch consists of only one switched valve device connected in series

3.4.8
cell
MMC building block where each switch position consists of more than one IGBT-diode pair connected in series

Note 1 to entry: See Figure A.13.

3.4.9
VSC valve level
smallest indivisible functional unit of VSC valve

Note 1 to entry: For any VSC valve in which IGBTs are connected in series and operated simultaneously, one VSC valve level is one IGBT-diode pair including its auxiliaries (see Figure A.13). For MMC type without IGBT-diode pairs connected in series one valve level is one submodule together with its auxiliaries (see Figure A.12).

3.4.10
diode valve level
part of a diode valve composed of a diode and associated circuits and components, if any

3.4.11
redundant levels
maximum number of series connected VSC valve levels or diode valve levels in a valve that may be short-circuited externally or internally without affecting the safe operation of the valve as demonstrated by type tests, and which if and when exceeded, would require shutdown of the valve to replace the failed levels or acceptance of increased risk of failures

Note 1 to entry: In valve designs such as the cascaded two level converter, which contain two or more conduction paths within each cell and have series-connected VSC valve levels in each path, redundant levels shall be counted only in one conduction path in each cell.

3.4.12
dynamic braking valve level
part of a dynamic braking valve comprising a controllable switch and an associated diode, or controllable switches and diodes connected in parallel, or controllable switches and diodes connected to a ~~half~~ bridge arrangement, together with their immediate auxiliaries, storage capacitor and energy dissipation resistors, if any

3.5 Valve structure terms

3.5.1
valve structure
structural components of a valve, required in order to physically support the valve modules

3.5.2
valve support
that part of the valve which mechanically supports and electrically insulates the active part of the valve from earth

3.5.3
multiple valve unit
MVU
mechanical arrangement of 2 or more valves or 1 or more VSC phase units sharing a common valve support

Note 1 to entry: A MVU might not exist in all topologies and physical arrangement of converters.

3.5.4
valve section
electrical assembly defined for test purposes, comprising a number of valve levels and other components, which exhibits pro-rated electrical properties of a complete valve

Note 1 to entry: For valves of controllable voltage source type the valve section shall include cell or submodule DC capacitor in addition to VSC valve levels.

Note 2 to entry: The minimum number of VSC or diode valve levels allowed in a valve section is defined along with the requirements of each test.

4 General requirements

4.1 Guidelines for the performance of type tests

4.1.1 Evidence in lieu

Each design of valve shall be subjected to the type tests specified in this document. If the valve is demonstrably similar to one previously tested, the supplier may, in lieu of performing a type test or individual parts of it, submit a test report of a previous type test for consideration by the purchaser. This should be accompanied by a separate report detailing the differences in the design and demonstrating how the referenced type test satisfies the test objectives for the proposed design. Conditions for use of evidence in lieu are listed in Table 1. 2

Table 1 – Conditions for use of evidence in lieu from another HVDC project

Type test	Clause	Conditions
Operational tests	6	• Equal or smaller number of valve levels to be tested • Same valve level design • Same valve electronics design • Identical or lower voltage stress and thermal stress[a] on each valve level
Dielectric tests on valve support structure	7	• Identical valve structure, including cooling pipes, cable paths, earthing system, if any • Same valve material and geometrical dimension • Equal or higher air clearance to valve hall and other related equipment inside the valve hall • Equal or lower voltage stress, including DC voltage stress, AC voltage stress and impulse voltage stresses
Dielectric tests on multiple valve unit	8	• Same MVU geometry between valves
Dielectric tests between valve terminals	9	• Identical valve structure, including cooling pipes, cable paths and earthing system, if any • Same valve material and geometrical dimension • Equal or lower voltage stress
IGBT overcurrent turn-off test	10	• Same valve level design • Same valve electronics design • Identical or lower prospective current stress
Short-circuit current test	11	• Same valve level design • Same short-circuit bypass components, if any, and function • Same valve electronics design • Identical or lower short-circuit current stress
Tests for valve insensitivity to electromagnetic disturbance	12	• Same as those indicated for Clauses 6 and 9
[a] Semiconductor devices thermal stress is a combined effect of current and cooling. Device thermal stress is characterised by the device junction temperature.		

4.1.2 Selection of test object

This subclause does not apply to tests on the valve supporting structure and multiple valve unit. The test object for those tests is defined in 7.2 and 8.3.

a) Type tests may be performed either on a complete valve or~~, in certain circumstances, on valve sections~~ MVU, or parts thereof, as indicated in Table 4.

b) The minimum number of valve levels to be operational type tested, depending on the valve levels in a single valve, is as shown in Table 2. This number applies to the type tests in Clauses 6, 10, 11 and 12. Those valve levels shall be tested in one test setup or multiple setups on several valve sections as defined in those clauses.

Table 2 – Minimum number of valve levels to be operational type tested as a function of the number of valve levels per valve

Number of valve levels, including redundant level per valve	Total number of valve levels to be tested
1 to 50	Number of valve levels in one valve
51 to 250	50
≥ 251	20 %

The minimum number of valve levels to be dielectric type tested can be equal to or lower than the number specified for the operational type test.

The minimum number of valve levels, however, shall be representative of the valve dielectric design.~~ Details can be found in 9.2.~~

c) Generally, the same valve sections are recommended to be used for all type tests. However, ~~with the agreement of the purchaser and supplier,~~ different tests may be performed on different valve sections in parallel, in order to speed up the programme for executing the tests. **3**

d) Prior to commencement of type tests, the valve, valve sections and/or the components of them ~~should~~ shall be demonstrated to have withstood the production tests to ensure proper manufacture.

4.1.3 Test procedure

The tests shall be performed in accordance with IEC 60060, where applicable with due account for IEC 60071 (all parts). Partial discharge measurements shall be performed in accordance with IEC 60270.

4.1.4 Ambient temperature for testing

The tests shall be performed at the prevailing ambient temperature of the test facility, unless otherwise specified.

4.1.5 Frequency for testing

AC dielectric tests can be performed at either 50 Hz or 60 Hz.~~ For Operational tests, specific requirements regarding the frequency for testing are given in the relevant clauses.~~ Operational tests shall be performed at the service frequency.

4.1.6 Test reports

At the completion of the type tests, the supplier shall provide type test reports in accordance with Clause 15.

4.1.7 Conditions to be considered in determination of type test parameters

Type test parameters ~~should~~ shall be determined based on the worst operating and fault conditions to which the valve can be subjected, according to system studies. Guidance on the conditions can be found in CIGRE Technical Brochure No. 447.

4.2 Atmospheric correction factor

When specified in the relevant clause, atmospheric correction shall be applied to the test voltages in accordance with IEC 60060-1. The reference conditions to which correction shall be made are the following:

– pressure:

- If the insulation coordination of the tested part of the valve is based on standard rated withstand voltages according to IEC 60071-1, correction factors are only applied for altitudes exceeding 1 000 m. Hence if the altitude of the site a_s at which the equipment will be installed is ≤1 000 m, then the standard atmospheric air pressure (b_0 = 101,3 kPa) shall be used with no correction for altitude. If a_s >1 000 m, then the standard procedure according to IEC 60060-1 is used except that the reference atmospheric pressure b_0 is replaced by the atmospheric pressure corresponding to an altitude of 1 000 m ($b_{1\ 000\ m}$).
- If the insulation coordination of the tested part of the valve is not based on standard rated withstand voltages according to IEC 60071-1, then the standard procedure according to IEC 60060-1 is used with the reference atmospheric pressure b_0 (b_0 = 101,3 kPa).

– temperature: design maximum valve hall air temperature (°C);

– humidity: design minimum valve hall absolute humidity (g/m^3).

Realistic worst-case combinations of temperature and humidity which can occur in practice shall be used for atmospheric correction.

The values to be used shall be specified by the supplier.

4.3 Treatment of redundancy

4.3.1 Operational tests

For operational tests, redundant valve levels shall not be short-circuited. The test voltages used shall be adjusted by means of a scaling factor k_n:

$$k_n = \frac{N_{tut}}{N_t - N_r}$$

where

N_{tut} is the number of series valve levels in the test object;

N_t is the total number of series valve levels in the valve;

N_r is the total number of redundant series valve levels in the valve.

4.3.2 Dielectric tests

For all dielectric tests between valve terminals, the redundant valve levels shall be short-circuited. The location of valve levels to be short-circuited shall be agreed by the purchaser and supplier.

NOTE Depending on the design, limitations ~~may~~ might be imposed upon the distribution of short-circuited valve levels. For example, there ~~may~~ might be an upper limit to the number of short-circuited valve levels in one valve section.

For all dielectric tests on valve section, the test voltages used shall be adjusted by means of a scaling factor k_0:

$$k_0 = \frac{N_{tu}}{N_t - N_r}$$

where

N_{tu} is the number of series valve levels not short circuit connected in the test object;

N_t is the total number of series valve levels in the valve;

N_r is the total number of redundant series valve levels in the valve.

4.4 Criteria for successful type testing

4.4.1 General

Experience in semiconductor application shows that, even with the most careful design of valves, it is not possible to avoid occasional random failures of valve level components during service operation. Even though these failures may be stress-related, they are considered random to the extent that the cause of failure or the relationship between failure rate and stress cannot be predicted or is not amenable to precise quantitative definition. Type tests subject valves or valve sections, within a short time, to multiple stresses that generally correspond to the worst stresses that can be experienced by the equipment not more than a few times during the life of the valve. Considering the above, the criteria for successful type testing set out below therefore permit a small number of valve levels to fail during type testing, providing that the failures are rare and do not show any pattern that is indicative of inadequate design and providing that the failed valve level permits the rest of the valve or valve section to continue operating without degraded performance.

4.4.2 Criteria applicable to valve levels

Criteria applicable to valve levels are as follows.

a) If, following a type test as listed in Clause 5, more than one valve level (alternatively more than 1 % of the tested valve levels, if greater) has become short or open circuited, then the valve shall be deemed to have failed the type tests.

b) If, following a type test, one valve level (or more if still within the 1 % limit) has become short or open circuited, then the failed level(s) shall be restored and this type test repeated.

c) If the cumulative number of short or open circuited valve levels during all type tests is more than 3 % of the tested valve levels, then the valve shall be deemed to have failed the type test.

d) The valve or valve sections shall be checked after each type test to determine whether or not any valve levels have become short or open circuited. Failed IGBT/diode or auxiliary components found during or at the end of a type test may be replaced before further testing.

e) At the completion of the test programme, the valve or valve sections shall undergo a series of check tests, which shall include as a minimum:

   – check for voltage withstand of valve levels;
   – check of the gating circuits;
   – check of the monitoring circuits;
   – check of any protection circuits forming an integral part of the valve;
   – check of the voltage grading circuits.

f) Valve levels short circuits occurring during the check tests shall be counted as part of the criteria for acceptance defined above. In addition to short or open circuited levels, the total number of valve levels exhibiting faults which do not result in valve level short circuit, which are discovered during the type test programme and the subsequent check test, shall not exceed 3 % of the number of tested valve levels in dielectric and operational type tests~~, whichever is lower~~. If the number of such levels exceeds 3 %, then the nature of the faults and their cause shall be reviewed and additional action, if any, agreed between purchaser and supplier.

g) When applying the percentage criteria to determine the permitted maximum number of short or open circuited valve levels and the permitted maximum number of levels with faults which have not resulted in a valve level becoming short or open circuited, it is usual practice to round off all fractions to the next highest integer, as illustrated in Table 3.

Table 3 – Valve level faults permitted during type tests

Number of valve levels tested	Number of valve levels permitted to become short or open circuited in any one type test	Total number of valve levels permitted to become short or open circuited in all type tests	Additional number of valve levels, in all type tests, which have experienced a fault but have not become short or open circuited
Up to 33	1	1	1
34 to 67	1	2	2
68 to 100	1	3	3
101 to 133 **4**	2	4	4
~~etc.~~			

The distribution of short or open circuited levels and of other valve level faults at the end of all type tests shall be essentially random and not show any pattern that may be indicative of inadequate design.

4.4.3 Criteria applicable to the valve as a whole

Breakdown of or external flashover across common electrical equipment associated with more than one valve level of the valve, or disruptive discharge in dielectric material forming part of the valve structure, cooling ducts, light guides or other insulating parts of the pulse transmission and distribution system shall not be permitted.

Component and conductor surface temperatures, together with associated current-carrying joints and connections, and the temperature of adjacent mounting surfaces shall at all times remain within limits permitted by the design.

5 List of type tests

Table 4 lists the type tests given in Clauses 6, 7, 8, 9, 10, 11 and 12.

Table 4 – List of type tests

Type test	Clause or subclause	Test object
Maximum continuous operating duty test	6.4	Valve or valve section
Maximum temporary over-load operating duty test	6.5	Valve or valve section
Minimum DC voltage test	6.6	Valve or valve section
Valve support DC voltage test	7.3.2	Valve support
Valve support AC voltage test	7.3.3	Valve support
Valve support switching impulse test	7.3.4	Valve support
Valve support lightning impulse test	7.3.5	Valve support
MVU DC voltage test to earth	8.4.1	MVU
MVU AC voltage test	8.4.2	MVU
MVU switching impulse test	8.4.3	MVU
MVU lightning impulse test	8.4.4	MVU
Valve AC – DC voltage test	9.4.1 or 9.4.2 **5**	Valve ~~(~~or valve section~~ if agreed between supplier and purchaser)~~
Valve switching impulse test	9.4.3.2	
Valve lightning impulse test	9.4.3.3	
IGBT overcurrent turn-off test	10	Valve or valve section
Short-circuit current test	11	Valve or valve section
Test for valve insensitivity to electromagnetic disturbance	12	Valve ~~(~~or valve section~~ if agreed between supplier and purchaser)~~
NOTE Valve section used in the valve AC–DC voltage test (9.4.1 or 9.4.2), valve switching impulse voltage test (9.4.3.2) and valve lightning impulse voltage test (9.4.3.3) should be a single structure representative of valve dielectric design.		

6 Operational tests

6.1 Purpose of tests

The principal objectives of the operational tests are:

a) to check the adequacy of the VSC/diode level and associated electrical circuits in a valve with regard to current, voltage and temperature stresses in the conducting state, at turn-on and turn-off under the worst repetitive stress conditions;

b) to demonstrate correct interaction between valve electronics and power circuits of the VSC valves.

6.2 Test object

The tests may be performed on either the complete valve or on valve sections. The choice depends mainly upon the valve design and the test facilities available. The tests specified in this clause are valid for valve sections containing five or more series-connected valve levels. If tests with fewer than five levels are proposed, additional test safety factors shall be agreed. Under no circumstances shall the number of series-connected levels for tests be less than three.

The valve or valve sections under test shall be assembled with all auxiliary components. ~~When required, a proportionally scaled valve arrester shall be included.~~ For the valves with valve surge arrester, a proportionally scaled valve arrester may be included.

The coolant shall be in a condition representative of service conditions. Flow and temperature, in particular, shall be set to the most unfavourable values appropriate to the test in question, such that the relevant component temperature(s) are equal to the values applicable in service.

6.3 Test circuit

For valve designs which act as a controllable voltage source and contain in-built DC capacitance, the DC capacitance and its connections to the semiconductor devices are an integral part of the test object.

However, for valve designs which function as switches, where the DC capacitor is separate from the valve, the DC capacitor needs to be correctly represented in the test circuit. In particular, the series stray inductance in the connections between the DC capacitor and the valve, and the stray capacitance across the valve section, shall be correctly reproduced and scaled to the size of valve section under test. Test circuit interconnections shall be of a type that is representative of the type used in the converter, in order not to introduce unrealistic levels of damping due to skin effects.

6.4 Maximum continuous operating duty test

The test needs to reproduce the following parameters based on the worst in service operating conditions of the converter. More than one test may be necessary to reproduce all parameters at their maximum values.

For VSC valves:

- maximum ~~continuous~~ steady-state IGBT junction temperatures;
- maximum ~~continuous~~ steady-state FWD junction temperatures;
- where snubbers are used, maximum ~~continuous~~ steady-state snubber component temperatures;
- maximum ~~continuous~~ steady-state turn-on and turn-off voltage and current.

For diode valves:

- maximum ~~continuous~~ steady-state diode junction temperature;
- where snubbers are used, maximum ~~continuous~~ steady-state snubber component temperatures;
- maximum ~~continuous~~ steady-state diode turn-off voltage and current.

All of these parameters need to be reproduced during the maximum continuous operating duty test. They may be reproduced either in separate tests or as a combined test.

The test voltage shall be based on the maximum continuous direct voltage, the test switching frequency shall be based on the maximum continuous switching frequency and the modulation pattern shall be representative of that used in service.

The test current, in RMS, shall be determined taking harmonic currents into account and any other additional currents through the valve.

The test current value shall incorporate a test safety factor of 1,05.

For switch type valve, the test voltage U_{tpv1} corresponding to the maximum continuous operating DC voltage shall be determined as follows: **6**

$$U_{tpv1} = U_{dmax} \times k_n \times k_1$$

where

U_{dmax} is the maximum continuous operating DC voltage of the valve, including ripple;

k_n is a test scaling factor according to 4.3.1;

k_1 is a test safety factor;

k_1 = 1,05.

For controllable voltage source type valve the test voltage, U_{tpvl1}, per valve level shall be determined as follows:

$$U_{tpvl1} = U_{cmax} \times k_1$$

where

U_{cmax} is the maximum continuous operating DC voltage of the valve level, including ripple;

k_1 is a test safety factor;

k_1 = 1,05.

The duration of the test shall be not less than 30 min after the exit coolant temperature has stabilized.

6.5 Maximum temporary over-load operating duty test

If the valve is specified for temporary over-load operation, a maximum temporary operating duty test shall be performed.

NOTE Capability of converter valves in a maximum temporary over-load operation is typically in a few seconds of time while valve cooling is unable to act.

The test conditions, where required, shall be determined using the same methodology as in 6.4 above. However, the test current shall be the specified over-load current without a test safety factor. 7

Prior to the test, the valve or valve section shall be brought to thermal equilibrium under the conditions of 6.4. The temporary operating duty test is then started from this initial condition and continued for a duration equal to the duration of the temporary overload multiplied by 1,2.

After the temporary over-load operation ~~duty test, 10 min maximum continuous operating duty test shall be performed~~ return to the conditions of maximum continuous operation as in 6.4 and maintain constant for 10 min.

6.6 Minimum DC voltage test

This test is to verify the correct performance of those valve designs in which energy for the valve electronic circuits is extracted from the voltage appearing between the valve terminals.

The test consists of applying a DC voltage between the terminals of the valve or valve section. For this test, only the voltage, not the current, is important.

The correct operation of the valve electronic circuits may be demonstrated either by deblocking the valve or valve section, or by remaining in the blocked state and monitoring the data back signals from the valve electronics.

The test voltage U_{min} is defined as:

$$U_{\text{min}} = \frac{N_{\text{tut}}}{N_{\text{t}}} \times U_{\text{W}} \times k_2$$

where

U_{W} is the lowest DC voltage across one valve in service operation where proper function of the valve electronics is required;

N_{tut} is the number of series-connected VSC levels under test;

N_{t} is the total number of series-connected VSC levels in a single valve, including redundancy;

k_2 is a test safety factor;

k_2 = 0,95.

The duration of test shall be not less than 10 min.

7 Dielectric tests on valve support structure

7.1 Purpose of tests

The principal objectives of these tests are:

a) to verify the voltage withstand capability of the insulation of the valve support, cooling ducts, light guides and other insulating components associated with the valve support. If there is insulation to earth other than the valve support, then additional tests may be necessary;

b) to verify that the partial discharge inception and extinction voltages are above the maximum operating voltage appearing on the valve support.

NOTE Depending upon the application, it ~~may~~ might be possible to eliminate some of the tests on the valve support, subject to agreement between purchaser and supplier.

7.2 Test object

The valve support to be used for the tests may be a representative separate object including representation of the adjacent parts of the valve or may form part of the assembly used for single valve or multiple valve unit tests. It shall be assembled with all ancillary components in place and shall have the adjacent earth potential surfaces properly represented. The proximity of adjacent earth potential surfaces (equipment or building infrastructure) shall be assessed, and representation included where appropriate. For clearances that are significantly greater than those determined by insulation co-ordination requirements, e.g. clearances driven instead by access requirements, then consideration may be given to omit earth potential surfaces in these locations. If a single valve consists of a single structure, then its large size may sometimes make it impractical to test the complete valve in a laboratory. In such cases it is permitted to perform the valve support structure tests on a pro-rated section of the support structure, provided it can be demonstrated that the design of the test object is representative of the design of the full structure and the tests cover the worst stresses experienced by any part of the valve support structure. 8

The coolant shall be in a condition representative of the most onerous service condition for the purpose of the test.

If a single valve consists of more than one structure such that there is more than one valve support structure per valve, then it shall be demonstrated that the tests proposed cover the worst stresses experienced by any of the valve support structures.

7.3 Test requirements

7.3.1 General

All test levels below are subject to atmospheric correction as described in 4.2.

7.3.2 Valve support DC voltage test

The two main terminals of the valve shall be connected together, and the DC voltage then applied between the two main terminals thus connected and earth. Starting from a voltage not higher than 50 % of the ~~maximum~~ 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage as fast as possible, kept constant for 1 min, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero. During the last hour of the specified 3 h test, the number of partial discharges exceeding 300 pC shall be recorded as described in IEC 60700-1:2015 and IEC 60700-1:2015/AMD1:2021, Annex B.

The number of pulses exceeding 300 pC shall not exceed 15 pulses per minute, averaged over the recording period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

~~NOTE 1 Where possible the test voltage should be increased from 50 % to the maximum voltage level within approximately 10 s. A longer time may be used; however, this may overstress the test object.~~

~~NOTE 2~~ If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity, the valve support may be short-circuited and earthed for a duration of several hours. The same procedure may be followed at the end of DC voltage test.

The valve support DC test voltage U_{tds} shall be determined in accordance with the following:

1 min test

$$U_{tds} = \pm U_{dmS1} \times k_3 \times k_t$$

3 h test

$$U_{tds} = \pm U_{dmS2} \times k_3$$

where

U_{dmS1} is the maximum ~~of 1 s average value of~~ short-duration voltage appearing across the valve support, as determined by insulation coordination studies. U_{dmS1} shall be the higher of (a) the highest voltage averaged over a 1 s period and (b) the average voltage during the time from the peak voltage to the time when the voltage decreases rapidly through the action of fast discharge devices or re-configuration, if any; **9**

U_{dmS2} is the maximum value of the DC component of the steady-state operating voltage appearing across the valve support;

k_3 is a test safety factor;

k_3 = 1,10 for 1 min test;

k_3 = 1,15 for 3 h test;

k_t is the atmospheric correction factor according to 4.2.

7.3.3 Valve support AC voltage test

To perform the test, the two main terminals of the valve shall be connected together, and the AC test voltage then applied between the two main terminals thus connected and earth.

Starting from a voltage not higher than 50 % of the ~~maximum~~ 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The valve support AC test voltage U_{tas} shall be determined in accordance with the following:

1 min test:

$$U_{tas} = \frac{U_{mS1}}{\sqrt{2}} \times k_4 \times k_t$$

30 min test

$$U_{tas} = \frac{U_{mS2}}{\sqrt{2}} \times k_4$$

where

U_{mS1} is the peak value of maximum voltage appearing on the valve support in service, particularly in system fault condition and valve fault operation condition. The overvoltage limiting effect of phase arrester or other overvoltage protection means, if any, shall be taken into account to derive this overvoltage;

U_{mS2} is the peak value of the maximum repetitive operating voltage across the valve support during steady-state operation, including switching overshoot;

k_4 is a test safety factor;

k_4 = 1,10 for 1 min test;

k_4 = 1,15 for 30 min test; **10**

k_t is the atmospheric correction factor according to 4.2.

7.3.4 Valve support switching impulse test

The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltages between the main terminals of the valve (connected together) and earth.

A standard switching impulse voltage wave shape in accordance with IEC 60060 shall be used.

The test voltage shall be selected in accordance with the insulation coordination of the VSC substation.

7.3.5 Valve support lightning impulse test

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltages between the main terminals of the valve (connected together) and earth.

A standard lightning impulse voltage wave shape in accordance with IEC 60060 shall be used.

The test voltage shall be selected in accordance with the insulation coordination of the VSC substation.

8 Dielectric tests on multiple valve unit

8.1 General

This clause is only applicable if more than one valve is installed in a common valve structure (multiple valve unit). In the case where each individual valve is mounted in a dedicated valve structure, this clause is not applicable.

8.2 Purpose of tests

The principal objectives of these tests are:

a) to verify the voltage withstand capability of the external insulation of the MVU, with respect to its surroundings, especially for the valve(s) connected at pole potential;

b) to verify the voltage withstand capability between single valves in a MVU structure;

c) to verify that the partial discharge levels are within specified limits.

8.3 Test object

There are many possible arrangements of valves and multiple valve units. The test object(s) shall be chosen to reflect, as accurately as possible, the service configuration of valves insofar as is necessary for the test in question. The test object shall be fully equipped unless it can be shown that some components can be simulated or omitted without reducing the significance of the results.

Individual valves may have to be short-circuited depending on the configuration of the MVU and the objectives of the test.

When the low-voltage terminal of the MVU is not connected to earth potential, care shall be taken to suitably terminate the low voltage terminal of the MVU during tests to correctly simulate the voltage appearing at this terminal. Earth planes shall be used, whose separation shall be determined by the proximity of other valves and earth potential surfaces.

8.4 Test requirements

8.4.1 MVU DC voltage test to earth

The DC test voltage shall be applied between the highest potential DC terminal of the MVU and earth.

Starting from a voltage not higher than 50 % of the ~~maximum~~ 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage as fast as possible, kept constant for 1 min, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

~~NOTE 1~~ Where possible the test voltage ~~should~~ shall be increased from 50 % to the ~~maximum~~ 1 min test voltage level within approximately 10 s. ~~A longer time may be used; however, this may overstress the test object.~~

During the last hour of the specified 3 h test, the number of partial discharges exceeding 300 pC shall be recorded.

The number of pulses exceeding 300 pC shall not exceed 15 pulses per minute, averaged over the recording period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC, and no more than one pulse per minute shall exceed 2 000 pC.

~~NOTE 2~~ If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity, the MVU terminals may be short-circuited together and earthed for a duration of several hours. The same procedure may be followed at the end of DC voltage test.

The MVU DC test voltage U_{tdm} shall be determined in accordance with the following:

1 min test

$$U_{tdm} = \pm U_{dmm1} \times k_5 \times k_t$$

3 h test

$$U_{tdm} = \pm U_{dmm2} \times k_5$$

where

U_{dmm1} is the maximum ~~of 1 s average value of~~ short-duration voltage appearing between the high-voltage terminal of MVU and earth, as determined by insulation coordination studies. U_{dmm1} shall be the higher of (a) the highest voltage averaged over a 1 second period and (b) the average voltage during the time from the peak voltage to the time when the voltage decreases rapidly through the action of fast discharge devices or re-configuration, if any; **9**

U_{dmm2} is the maximum value of the DC component of the steady-state operating voltage appearing between the high-voltage terminal of the MVU and earth;

k_5 is a test safety factor;

k_5 = 1,10 for 1 min test;

k_5 = 1,15 for 3 h test;

k_t is the atmospheric correction factor according to 4.2.

8.4.2 MVU AC voltage test

If a MVU experiences AC or composite AC plus DC voltage stresses between any two terminals, the withstand capability of which is not adequately demonstrated by other tests, then it will be necessary to perform an AC voltage test between these terminals of the MVU.

To perform the test, the test voltage source shall be connected to the pair of MVU terminals in question. The point of earth connection is dependent on the test circuit arrangement.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, then reduced to the 30 min value, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The MVU AC test voltage U_{tam} shall be determined in accordance with the following:

1 min test

$$U_{\text{tam}} = \frac{U_{\text{mm1}}}{\sqrt{2}} \times k_6 \times k_{\text{t}}$$

30 min test

$$U_{\text{tam}} = \frac{U_{\text{mm2}}}{\sqrt{2}} \times k_6$$

where

U_{mm1} is the peak value of maximum voltage between the terminals of the MVU in service, particularly in system fault condition and valve fault operation condition. The overvoltage limiting effect of phase arrester or other overvoltage protection means, if any, shall be taken into account to derive this overvoltage;

U_{mm2} is the peak value of the maximum repetitive operating voltage between the terminals of the MVU during steady-state operation, including switching overshoot;

k_6 is a test safety factor;

k_6 = 1,10 for 1 min test;

k_6 = 1,15 for 30 min test; **10**

k_{t} is the atmospheric correction factor according to 4.2.

8.4.3 MVU switching impulse test

A standard switching impulse voltage waveshape in accordance with IEC 60060 shall be used.

The MVU switching impulse test voltage shall be applied between the high voltage terminal of the MVU and earth.

The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltage of a specified amplitude.

The MVU switching impulse test voltage U_{tsm} shall be determined in accordance with the following:

~~$U_{\text{tsm}} = \pm SIPL_{\text{m}} \cdot k_7 \cdot k_{\text{t}}$~~

$$U_{\text{tsm}} = \pm U_{\text{SIPL\_m}} \times k_7 \times k_t$$

where

~~*SIPL*~~$_{\text{m}}$ $U_{\text{SIPL\_m}}$ is the switching impulse protective level determined by insulation coordination taking into account the arrester(s) connected between the MVU high voltage terminal and earth;

k_7 is a test safety factor;

k_7 = 1,10;

k_{t} is the atmospheric correction factor;

k_{t} is the value according to 4.2.

If the test prescribed above does not adequately test the switching impulse withstand between all terminals of the MVU, then consideration shall be given to performing extra tests to check the insulation.

NOTE Subject to agreement between the purchaser and supplier, the MVU switching impulse test need not be performed if it can be shown by other means that:

a) the external air clearances to other valves and to earth are adequate for the switching impulse voltage withstand level required, and

b) the switching impulse withstand between any two terminals of the MVU is adequately demonstrated by other tests.

8.4.4 MVU lightning impulse test

A standard lightning impulse voltage wave shape in accordance with IEC 60060 shall be used.

The MVU lightning impulse test voltage shall be applied between the high voltage terminal of the MVU and earth.

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltage of specified amplitude.

The MVU lightning impulse test voltage U_{tlm} shall be determined in accordance with the following:

~~$U_{\text{tlm}} = \pm LIPL_{\text{m}} \quad k_8 \quad k_{\text{t}}$~~

$$U_{\text{tlm}} = \pm U_{\text{LIPL\_m}} \times k_8 \times k_t$$

where

~~*LIPL*~~$_{\text{m}}$ $U_{\text{LIPL\_m}}$ is the lightning impulse protective level determined by insulation co-ordination, taking into account the arrester(s) connected between the MVU high voltage terminal and earth;

k_8 is a test safety factor;

k_8 = 1,10;

k_{t} is the atmospheric correction factor;

kt is the value according to 4.2.

If ~~it cannot be demonstrated that~~ the test prescribed above does not adequately test the lightning impulse withstand voltage between all terminals of the MVU, then consideration shall be given to performing extra tests to check this insulation.

NOTE Subject to agreement between the purchaser and supplier, the MVU lightning impulse test need not be performed if it can be shown by other means that:

a) the external air clearances to other valves and to earth are adequate for the lightning impulse voltage withstand level required, and

b) the lightning impulse withstand voltage between any two terminals of the MVU is adequately demonstrated by other tests.

9 Dielectric tests between valve terminals

9.1 Purpose of the test

These tests are intended to verify the design of the valve regarding its voltage-related characteristics for various types of overvoltages (DC, AC, switching impulse and lightning impulse overvoltages). The tests ~~should~~ shall demonstrate that:

a) the valve will withstand the specified overvoltages;

b) partial discharges will be within specified limits under specified test conditions;

c) the internal voltage grading circuits, if any, have sufficient power rating~~;~~

~~d) the valve electronic circuits behave as expected~~.

It should be noted that the tests described in this clause are based on standard wave shapes and standard test procedures as developed for the testing of high-voltage AC systems and components. This approach offers great advantages to the industry because it allows much of the existing technology of high-voltage testing to be carried over to the qualification of HVDC valves. On the other hand, it must be recognized that a particular HVDC application may result in wave shapes different from the standards and, in this case, the test may be modified so as to realistically reflect expected conditions.

It should be also noted that the atmospheric correction is not needed in dielectric tests between valve terminals if the site altitude is less than 1 000 m. However, for valves installed at an altitude exceeding 1 000 m the valve internal air clearance shall be verified by additional tests under the atmospheric corrected test voltages. IGBT-diode pairs can be replaced by insulating blocks in these tests. **11**

9.2 Test object

For valves of the switch type, the test object should generally be a complete valve. For valves of the controllable voltage source type, testing a complete valve might not be practical because of its large physical size. In such cases the test object should generally be a single structure representative of valve dielectric design. Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections, under test conditions, is representative of the voltage distribution within a complete valve in service. The test valve or valve section shall be assembled with all auxiliary components except for the valve arrester if provided. The valve may form part of a multiple valve unit.

~~For all impulse tests, the valve electronics shall be energized unless otherwise specified.~~ **12**

If a valve section is used as the test object, the minimum number of valve levels in the test section ~~should~~ shall be agreed by the purchaser. In such cases, additional tests to verify the insulation between different parts of the complete valve may be needed and shall be agreed between purchaser and supplier.

The coolant shall be in a condition that represents service conditions except for flow rate which can be reduced. If any object external to the structure is necessary for proper representation of the stresses during tests, it shall be included or simulated in the test. ~~Earth planes shall be used, whose separation shall be determined by the proximity of other adjacent valves and earth potential surfaces.~~ The proximity of adjacent earth potential surfaces (equipment or building infrastructure) shall be assessed, and representation included where appropriate. For clearances that are significantly greater than those determined by insulation coordination

requirements, e.g. clearances driven instead by access requirements, then consideration may be given to omit earth potential surfaces in these locations.

~~The test object used for the valve dielectric tests will normally not permit the application of atmospheric correction to the specified test voltages without overstressing the internal components. For this reason, no atmospheric correction factor is applied to any of the dielectric tests between valve terminals. The supplier shall demonstrate that the effects of atmospheric conditions on the valve internal withstand have been allowed for adequately.~~

9.3 Test methods

9.3.1 General

VSC valves differ from line commutated converter (LCC) valves and other high-voltage equipment in several aspects. One of the most important differences is that the converter contains very large capacitive energy storage. For valves of the controllable voltage-source type, the storage is an integral part of the valve while for switch-type valves it is closely connected to the valve. The second major difference is the active voltage control at individual VSC valve levels. As a result of these characteristics, the test method used in LCC valve dielectric tests cannot be applied to such valves. **13**

Performing the valve dielectric test presents considerable practical difficulties on controllable voltage source type VSC valves because of the high current drawn by those in-built capacitances. ~~For this reason, following valve dielectric test methods are acceptable.~~ The very limited current ratings of available test supplies in practical high-voltage test laboratories mean that, without modifying the test object, an excessively long time is required to charge up the capacitance of the test object to the required voltage during the AC–DC voltage test, and this unreasonably over-stresses the test object. The very large capacitance also makes measurement of partial discharges impossible, and impulse voltages between the valve terminals do not occur on a deblocked valve during operation. For this reason, two valve dielectric test methods, on the same principle, are defined for controllable voltage source type valve dielectric tests. Supplier can use either of them for the valve dielectric test.

Valve dielectric test on switch type VSC valves shall follow Method one.

9.3.2 Method one

Temporary substitution of a special test capacitor with reduced capacitance but the same ~~physical size test capacitor is permissible~~ housing as the original capacitor in each valve level is necessary if this method is used in test of controllable voltage source type valves **14**. This test capacitor shall allow a test voltage build-up across the test object during test.

In addition, it may be necessary to disable gate electronics or other auxiliary circuits in this test or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

When gate electronics or other auxiliary circuits are disabled for the 10 s test, the active voltage control function, if any, provided by gate electronics or other auxiliary circuits on each IGBT level may be represented by other means, for example, high resistance shunt resistors across test IGBT levels for appropriate voltage sharing.

If it is not possible to disable gate electronics or other auxiliary circuits in this test and interference can be proven to be caused by electronics circuit, then this interference may be deducted from measurement.

9.3.3 Method two 15

Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections under test conditions, is representative of the voltage distribution within a complete valve in service.

In case of a controllable voltage source type VSC valve the active control of sub-module capacitor voltages equalises the voltage distribution across the complete valve. The in-built capacitances react as constant voltage sources with very low internal impedance. An impulse voltage will drive a high current, the resulting change of the sub-module voltage follows the tolerance of the in-built capacitor.

Valve dielectric test is done ~~by two~~ in single steps. Step one focuses on the component level and step two on the valve or valve section. ~~In step one, module levels are tested independently.~~

In step one, valve levels are tested independently. Insulation and partial discharge tests with AC, DC and/or combined AC–DC voltage shall be performed on sub-component level (e.g. without power module electronics activated and without capacitor) or on full submodule level. The aim is to demonstrate both the insulation withstand capability for every single sub-component and freedom from partial discharge for every sensitive point within the valve level.

As stated, the even distribution by actively controlled sub-module voltages allows to perform the dielectric test between valve terminals and also between tiers with adjusted test voltage levels.

Consequently, in step two, the test is done with submodule levels short-circuited, interconnections between adjacent submodules removed, and valve or valve section voltage distribution controlled by an external grading circuit, for example a resistor array, capacitor array or RC array.

~~Atmospheric correction to the specific test voltages can be added in step two.~~

The inter-tier structure represents a typical section of the tower structure. Essential components of the tower structure are exposed to the specified voltage values and shapes. Test of air clearance and creepage distances of tier insulators and capacitor's housing, fibre optics including their ducts, water cooling pipes and mechanical design. AC, DC (both including PD measurement) and impulse voltages will be tested. Additional safety margin to the specific test voltages is possible and used, e.g. atmospheric correction to the specific test voltages can be added.

NOTE The addition of external grading networks could modify the profile of the test object such that it is not fully representative of in-service equipment. Practically this could lead to difficulties in performing the test, especially in determining sources of partial discharge. Hence an alternative method can be used instead of fitting grading networks, where each insulation gap is tested independently at voltages relevant to each particular gap. This can be achieved by a combination of either removing interconnections and/or shorting out relevant parts of the test object, then applying the equivalent scaled voltage across the gap. The test is performed once for each design of insulation gap e.g. inter-tier, inter-stack, inter-sub-module. Where appropriate in the design, the test set-up also needs to consider diagonal gaps (gaps between sub-modules belonging to different stacks and different tiers, one above the other).

9.4 Test requirements

9.4.1 ~~Valve~~ Composite AC-DC voltage test 16

~~This test consists of a short-duration test and a long-duration test. The short-duration~~ This test reproduces the composite AC-DC voltage resulting from certain converter or system faults and in steady-state operation. The test consists of a short-duration test and a long-duration test.

In this test, a capacitor can be used in conjunction with an AC test voltage source to produce a composite AC-DC voltage waveform. Depending on the converter topology, the capacitor could

be an integral part of the valve, or it could be a separate item (part of the test circuit, not part of the test object).

Alternatively, a separate DC voltage source could be used to substitute the capacitor.

Starting from a voltage not higher than 50 % of the ~~maximum~~ 10 s test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For AC PD (partial discharge) measurement, the ~~peak value~~ level of ~~the periodic~~ partial discharge recorded during the last minute of the 3 h test shall be less than 200 pC, provided that the components which are sensitive to partial discharge in the valve have been separately tested. For DC PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

NOTE 1 If an increasing trend in the rate or magnitude of partial discharge is observed, the test duration ~~may~~ might be extended by mutual agreement between the purchaser and supplier.

NOTE 2 It may be necessary to disable gate electronics or other auxiliary circuits in this test, or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

The valve test voltages have a sinusoidal waveshape superimposed on a DC level.

The valve 10 s test voltage U_{tv1} shall be determined in accordance with the following: **17**

$$U_{tv1} = \left(k_{c1} \cdot U_{tac1} \cdot \sin(2\pi ft) + U_{tdc1}\right) \cdot k_o \cdot k_9$$

$$U_{tv1} = \left(k_{c1} \times U_{tac1} \times \sin\left(2\pi ft\right) + U_{tdc1}\right) \times k_0 \times k_9$$

where

~~U_{ac1} is the peak value of maximum transient a.c. component over-voltage across valve. The limiting effect of valve arrester or pole arrester can be taken into account to derive the over-voltage in service condition;~~

U_{tac1} is the peak value of the AC component of maximum temporary overvoltage appearing between the terminals of the valve, calculated from the peak-to-peak valve voltage divided by two;

~~U_{dc1} is the maximum transient d.c. component over-voltage across valve. The limiting effect of valve arrester or pole arrester can be taken into account to derive the over-voltage in service condition;~~

U_{tdc1} is the maximum of 1 s average value of the DC component of voltage appearing between the terminals of the valve at faults, after taking into account of voltage limiting effect of DC pole surge arrester;

k_{c1} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define ~~Uac1~~ U_{tac1}. For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

k_0 is a test scaling factor according to 4.3.2;

k_9 is a test safety factor;

k_9 = 1,1;

f is the test frequency (50 Hz or 60 Hz depending on test facilities).

NOTE 3 The conditions leading to the highest values of U_{tac1} and U_{tdc1} might not occur simultaneously. When performing a combined AC–DC test it is important to use self-consistent conditions that lead to the worst combined valve stress, in order to avoid over-stressing, the test object. For the 10 s test, the most important parameter is generally the peak of the combined voltage.

The valve 3h test voltage U_{tv2} shall be determined in accordance with the following:

~~$$U_{tv2} = U_{tac2} + U_{tdc2}$$~~

~~$$U_{tac2} = \frac{\sqrt{2} \cdot U_{max-cont} \cdot \sin(2\pi ft)}{\sqrt{3}} k_{c2} k_o k_{10}$$~~

~~$$U_{tdc2} = U_{dmax} k_o k_{10}$$~~

~~where~~

~~$U_{max-cont}$ is the maximum steady-state phase-to-phase voltage on the a.c. system or the valve side of the transformer, if a converter transformer is used in between a.c. system and converters;~~

~~U_{dmax} is the maximum value of the d.c. component of the steady-state operating voltage of the d.c. system;~~

~~k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2};~~

~~k_o is a test scaling factor according to 4.3.2;~~

~~k_{10} is a test safety factor;~~

~~k_{10} = 1,10;~~

~~f is the test frequency (50 Hz or 60 Hz depending on test facilities).~~

$$U_{tv2} = U_{tac2} + U_{tdc2}$$

$$U_{tac2} = U_{max-cont} \times \sin(2\pi ft) \times k_{c2} \times k_0 \times k_9$$

$$U_{tdc2} = U_{dmax} \times k_0 \times k_9$$

where

$U_{max-cont}$ is the peak value of the AC component of steady-state voltage appearing between the terminals of the valve, calculated from the peak-to-peak valve voltage divided by two;

U_{dmax} is the maximum value of the DC component of the steady-state operating voltage between the terminals of the valve, calculated from the voltage between the DC terminals of the converter divided by two;

k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2}. For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

f is the test frequency (50 Hz or 60 Hz depending on test facilities).

9.4.2 Alternative tests (Method 2 only) 18

9.4.2.1 General

When method two is adopted, the composite AC-DC voltage test specified in the previous sub-clause may be replaced, during step two, by an AC voltage test and an DC voltage test performed separately.

NOTE It is generally only possible to apply the alternative test method when testing passive insulation gaps, since the freewheel diodes in the valve will normally prevent the application of a pure AC voltage.

9.4.2.2 Valve AC voltage test

The test consists of applying the specified test voltages U_{tac1} and Ut_{ac2} for the specified duration. U_{tac1} and U_{tac2} have sinusoidal waveshapes with a frequency of 50 Hz or 60 Hz, depending on the test facility.

The test will be done with a short duration of 10 s and a long duration of 30 min.

Starting from a voltage not higher than 50 % of the 10 s test voltage, the voltage shall be raised to the specified 10 s test level, kept constant for 10 s, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero. Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The RMS value of valve 10 s AC test voltage, U_{tac1}, and 30 min AC test voltage, U_{tac2}, shall be determined in accordance with the following:

$$U_{tac1} = \frac{U_{vp1}}{\sqrt{2}} \times k_{c1} \times k_0 \times k_{10}$$

$$U_{tac2} = \frac{U_{vp2}}{\sqrt{2}} \times k_{c1} \times k_0 \times k_{10}$$

where

U_{vp1} is the peak value of the maximum temporary overvoltage across the valve;

U_{vp2} is the peak value of the maximum steady-state voltage across the valve;

k_{c1} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac1}. For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2}; For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

k_0 is the test scaling factor according to 4.3.2;

k_{10} is a test safety factor;

k_{10} = 1,10.

9.4.2.3 Valve DC voltage test

The test consists of applying the specified test voltages U_{tdc1} and U_{tdc2} for the specified duration.

The test will be done with a short duration of 10 s and a long duration of 3 h.

Starting from a voltage not higher than 50 % of 10 s test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For DC PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

The valve 10 s DC test voltage, U_{tdc1}, and 3 h DC test voltage, U_{tdc2}, shall be determined in accordance with the following:

$$U_{tdc1} = U_{vp1} \times k_0 \times k_{10}$$

$$U_{tdc2} = U_{vp2} \times k_0 \times k_{10}$$

9.4.3 Valve impulse tests ~~(general)~~

9.4.3.1 General

The following ~~should~~ shall be taken into account during valve impulse tests.

a) For some applications, for instance no overhead line is present in DC side and the busbar between phase reactor and valves is completely protected against direct lightning strike in AC side or in topologies, where the valve acts as a controllable voltage source with its own inbuilt DC capacitance, the valve impulse tests are less important since the valves do not see impulses at an amplitude which could be decisive in the electric performance of valves. Impulse tests in such applications can be omitted. **19**

NOTE 1 Unless all equipment between the transformer and DC reactors are completely enclosed, the possibility of lightning striking an exposed section of busbar adjacent to the valve (for example between the valve reactors and the valve) cannot be excluded. However, taking into account the small area affected and the low probability of having a lightning impulse of magnitude low enough to evade the shielding, this event is extremely unlikely to occur in practice and can therefore be ignored.

NOTE 2 The emergency turn-off of the IGBT valve while it is carrying current (IGBT overcurrent turn-off test: Clause 10) can also generate a transient overvoltage between the terminals of the valve. Part of this overvoltage appears directly across the valve levels and is covered by the IGBT overcurrent turn-off test but there might, in addition, be a transient voltage developed across the stray inductance of the busbars through the valve which might need to be considered in the assessment of impulse voltage stresses between terminals.

b) The impulse test will be applied only in one polarity which corresponds to the polarity of valve withstand voltage.

c) If the valve impulse withstand levels are equal to or less than the valve AC-DC test level, it is deemed that the valve AC-DC test can cover the impulse tests and consequently the impulse tests can be omitted.

9.4.3.2 Valve switching impulse test

A standard switching impulse voltage waveshape in accordance with IEC 60060 shall be used.

The test shall comprise three applications of switching impulse voltages of specified amplitude on the valve.

The valve switching impulse test withstand voltage U_{tsv} shall be determined in accordance with the following:

– Valve with valve arrester protection:

~~$U_{tsv} = SIPL_v \cdot k_0 \cdot k_{11}$~~

$$U_{tsv} = U_{SIPL\_v} \times k_0 \times k_{11}$$

where

~~$SIPL_v$~~ U_{SIPL_v} is the switching impulse protective level of valve arrester or protection level derived from AC and DC side arresters;

k_0 is a test scaling factor according to 4.3.2;

k_{11} is a test safety factor;

k_{11} = 1,10.

– Valve without valve arrester protection:

This test is intended to verify the valve insulation when the valve is not directly protected by surge arresters.

$$U_{tsv} = U_{cms} \times k_0 \times k_{12}$$

where

U_{cms} is the switching impulse prospective voltage across valve terminals according to system insulation coordination studies;

k_0 is a test scaling factor according to 4.3.2;

k_{12} is a test safety factor;

k_{12} = 1,15.

The valve shall withstand the test voltage without switching or insulation breakdown.

9.4.3.3 Valve lightning impulse test

A standard lightning impulse voltage waveshape in accordance with IEC 60060 shall be used.

The test shall comprise three applications of impulse voltages of specified amplitude on the valve.

The valve lightning impulse withstand voltage U_{tlv} shall be determined in accordance with the following.

– Valve with valve surge arrester protection:

~~$U_{tlv} = LIPL_v \cdot k_0 \cdot k_{13}$~~

$$U_{tlv} = U_{LIPL\_v} \times k_0 \times k_{13}$$

where

~~$LIPL_V$~~ U_{LIPL_v} is the lightning impulse protective level of the valve arrester or protection level derived from AC and DC side arresters;

k_0 is a test scaling factor according to 4.3.2;

k_{13} is a test safety factor;

k_{13} = 1,10.

– Valve without valve surge arrester protection:

This test is intended to verify the valve insulation when the valve is not directly protected by surge arresters.

$$U_{tlv} = U_{cml} \times k_0 \times k_{14}$$

where

U_{cml} is the lightning impulse prospective voltage across valve terminals according to system insulation coordination studies;

k_0 is a test scaling factor according to 4.3.2;

k_{14} is a test safety factor;

k_{14} = 1,15.

The valve shall withstand the test voltage without switching or insulation breakdown.

10 IGBT overcurrent turn-off test

10.1 Purpose of test

The principal objective is to check the adequacy of the VSC valve design, especially the IGBT, and the associated electrical circuits with regard to current and voltage stresses at turn-off in the event of certain short circuit faults or misfiring events.

The test shall replicate the worst combination of voltage stress and instantaneous junction temperature, based on conditions that represent the most unfavourable tolerance settings of the monitoring/protection circuits. Depending on the control and protection strategy more than one test may be required in order to reproduce all relevant stresses.

General requirements related to the test circuit and the representation of DC capacitor, loop stray inductance, etc. are as stated in 6.3.

10.2 Test object

The test object is as described in 6.2. However, it ~~shall~~ is also ~~be~~ necessary to represent certain protection or monitoring circuits if these are essential for the detection of an overcurrent event. For controllable voltage source type VSC valves, this test may also be performed on valve level. **20**

10.3 Test requirements

The test consists of operating the test object to thermal equilibrium under the conditions which lead to the highest steady-state junction temperature of the relevant IGBT (see 6.4) and then initiating an overcurrent event. The control and protection system then detects the overcurrent and suppresses the overcurrent by turning off the IGBTs at a current below the maximum safe turn-off limit.

For switch type valve, the test voltage U_{tpv2} ~~corresponding to the maximum temporary d.c. over-voltage~~ shall be determined as follows:

$$U_{tpv2} = U_{dtemp} \times k_n \times k_{15}$$

where

U_{dtemp} is the maximum temporary DC overvoltage of the valve, including ripple;

k_n is a test scaling factor according to 4.3.1;

k_{15} is a test safety factor;

k_{15} = 1,05.

~~The test current waveform in the time interval between detection of the overcurrent and the instant of turn-off of the IGBTs should be representative of the service condition, particularly in terms of current rate-of-rise di/dt.~~

For controllable voltage source type valve, the test voltage U_{tpvl2} per valve level shall be determined as follows: **6**

$$U_{tpvl2} = U_{ctemp} \times k_{15}$$

where

U_{ctemp} is the maximum temporary DC overvoltage per valve level, including ripple;

k_{15} is a test safety factor;

k_{15} = 1,05.

The rate-of-rise di/dt of the overcurrent shall be taken into consideration in the test to show that the control and protection system is able to turn-off the IGBTs fast enough before maximum safe turn-off limits are reached. This consideration can be shown either by increasing the rate-of-rise di/dt of the test current waveform if the test circuit allows for it or by increasing the protection level by taking into consideration of the total inherent delay in the control and protection system. **21**

11 Short-circuit current test

11.1 Purpose of tests

The principal objective is to check the adequacy of the devices, especially the diodes, any additional components used to protect the diodes (such as bypass thyristors) and the associated electrical circuits with regard to current stresses under specified short circuit conditions, such as short-circuit fault at DC side, until the control and protection circuit breaks the fault current. The VSC valves shall be designed to withstand the short circuit overcurrent for the number of cycles needed to open the main AC circuit breaker, without any failure or damage in the equipment, considering also that a possible recovery voltage could appear. ~~The test shall normally be performed with the valve electronics initially energized, unless the short-circuit current can occur under conditions where the valve is de-energized (For example due to the inrush current when the converter breaker is closed at start-up).~~ Valve electronics shall normally be energized for the part of the fault event where any actions are taken by it. For example, when blocking the IGBTs or turning on protective devices such as bypass thyristors. For other parts of the fault event, it is not necessary to energize the valve electronics. **22**

11.2 Test object

The test object is as described in 6.2.

11.3 Test requirements

The test consists of operating the test object to thermal equilibrium under the conditions which lead to the highest steady-state junction temperature of the relevant semiconductor component (see 6.4) and then initiating a fault current event. In order to define the maximum junction temperature rise of the IGBTs and the diodes, all the possible overload conditions (in terms of amplitude and duration) shall be taken into consideration.

The fault current amplitude, duration and the number of cycles shall be the maximum values expected in the actual field operation.

Alternative test waveform may be used, provided that the amplitude and energy accumulation are representative of those in fault conditions.

Where the test object experiences a recovery voltage between cycles of fault current, then this recovery voltage, including commutation overshoot where applicable, shall also be reproduced during the test. A test safety factor of 1,05 is applied to the recovery voltage.

Considering the difficulty in test laboratory to perform this test in generation of the recovery voltage between cycles of fault current, this test may, subjected to the agreement between purchaser and ~~manufacturer~~ supplier, be performed on component level.

12 Tests for valve insensitivity to electromagnetic disturbance

12.1 Purpose of tests

The principal objective is to demonstrate the insensitivity of the valve to electromagnetic interference (electromagnetic disturbance) arising from voltage and current transients generated within the valve and imposed on it from the outside. The sensitive elements of the valve are generally electronic circuits used for controlling, protection and monitoring of the valve levels.

Generally, the valve insensitivity to electromagnetic disturbance can be checked by monitoring the valve during other type tests. Of these, ~~the valve and~~ the valve maximum continuous operating duty test and maximum temporary overload operating duty test (see 6.4 and 6.5), the valve impulse tests (see 9.4.3) and the IGBT overcurrent turn-off test (see Clause 10) are the most important.

The tests shall demonstrate that:

a) out-of-sequence or spurious switching of IGBT does not occur;

b) the electronic protection circuits installed in the valve operate as intended;

c) false indication of valve level faults or erroneous signals sent to the converter control and protection systems by the valve base electronics, arising from receipt of false data from the valve monitoring circuits, does not occur.

NOTE For this document, tests to demonstrate valve insensitivity to electromagnetic disturbance apply only to the VSC valve and that part of the signal transmission system that connects the valve to earth. Demonstration of the insensitivity to electromagnetic disturbance of equipment located at earth potential and characterization of the valve as a source of electromagnetic disturbance for other equipment are not within the scope of this document.

12.2 Test object

Generally, the test object is the valve or valve sections as used for other tests.

When insensitivity to electromagnetic disturbance arising from coupling between adjacent valves in a MVU is to be demonstrated, two approaches are acceptable as defined in 12.3. In this case, the test object will be a separate valve or valve section according to the approach adopted.

12.3 Test requirements

12.3.1 General

When demonstrating insensitivity to electromagnetic disturbance arising from coupling between adjacent valves of a MVU, the test requirements depend on which of the two recommended approaches is adopted.

~~NOTE~~ The specific geometric arrangement to be used and the magnitude of the forward voltage for the electromagnetic disturbance test object ~~should be agreed, based on the design of MVU~~ shall be representative of the service conditions.

12.3.2 Approach one

Approach one is to simulate the source of electromagnetic disturbance directly as part of a test set-up. Such a test set-up will require more than one valve or valve section in order to check for interaction between them. The geometric arrangements of the source of the electromagnetic disturbance with respect to the valve under test shall be as close as possible to the service arrangement (or worse from an electromagnetic disturbance point of view). The electronics of the electromagnetic disturbance test object shall be energized. Those parts of the valve base electronics that are necessary for the proper exchange of information with the electromagnetic disturbance test object shall be included.

12.3.3 Approach two

Approach two is to determine the intensity of electromagnetic fields under worst operational conditions, either from theoretical considerations or by measurements. In a second step, these fields are simulated by a test circuit which generates correct (or worse) electromagnetic radiation at the respective frequencies. A valve section is then exposed to the fields generated by the test source.

An essential prerequisite to approach two is the determination of the dynamic field strength and direction at key locations in the valve. This can generally be obtained from search coil measurements taken during firing tests on a single valve. Alternatively, the field can be predicted from three-dimensional field modelling programs. A valve section shall then be tested using a separate field coil to produce field intensity, frequency content and direction which is at least as severe as the predicted values.

The following conditions for the valve section under test shall be met:

– the valve section shall have operational voltage (proportionally scaled) between its terminals and be forward biased at the time of energization of the field coil;
– the electronics of the valve section under test shall be energized;
– those parts of the valve base electronics that are necessary for the proper exchange of information with the valve section shall be included.

12.3.4 Acceptance criteria

The criteria for acceptance for both approaches one and two shall be as defined in 12.1.

13 Tests for dynamic braking valves

In some VSC HVDC schemes, but particularly where the HVDC system is exporting power from a small islanded AC system with little or no load (for example an offshore wind farm) the HVDC system may be required to include a dynamic braking system, for example as a chopper connected to the DC terminals of the VSC system. The function of the dynamic braking system is to absorb and dissipate the power generated in the islanded AC system during faults in the receiving-end AC system, typically for durations of 1 s to 2 s.

There are several possible ways of implementing such a dynamic braking system but the valves in this system will, in general, be of similar design to the main VSC valves used for power transmission.

The dynamic braking valves may require type tests, for which the requirements given in the preceding Clauses 6 to 12 are generally applicable; however, the dynamic braking valves generally require only a sub-set of the type tests applicable to VSC valves.

The dynamic braking valve normally remains in the standby state but is required to operate and carry current for short durations when the receiving-end AC system suffers a fault. The dielectric test conditions are therefore similar to those for the VSC valve but the operational test conditions only need to be applied for short durations.

NOTE 1 Subclause 4.1.1, *Evidence in lieu*, is applicable when the same valve design is used in both VSC valve and dynamic braking valve.

NOTE 2 For dynamic braking valve with a design of distributed on-built resistors or energy absorber element the operational duties can be done on site, due to the power limitation of test laboratory.

14 Production tests

14.1 General

This clause covers tests on assemblies of components that are parts of valves, valve sections, or auxiliary circuits for their protection, control and monitoring. It does not cover tests on individual components that are used within the valve, the valve support, or valve structure.

For valve component fault tolerance, information is provided in Annex B.

14.2 Purpose of tests

The purpose of the production tests is to verify proper manufacture by demonstrating that:

– all components and subassemblies used in the valve have been correctly installed in accordance with the design;
– the valve equipment functions as intended and predefined parameters are within prescribed acceptance limits;
– the valve sections and IGBT-diode pair levels (as appropriate) have adequate voltage withstand capability;
– consistency and uniformity in production is achieved.

14.3 Test object

All valve sections or parts thereof manufactured for the project shall be subjected to the routine production tests. The tests may be performed on valve sections or individual levels as appropriate to the design and available test facilities.

14.4 Test requirements

Uniformity in the specified production tests of different suppliers is unnecessary. The production tests shall take into account the special design characteristics of the valve and its components, the extent to which the components are tested prior to assembly, and the particular manufacturing procedures and techniques are involved. In this clause, only production test objectives are given.

In all cases, the supplier shall submit, for approval by the purchaser, a detailed description of the test procedures proposed to meet the production test objectives.

The minimum requirements for routine production tests are listed in 14.5. The order in which the tests are listed implies neither ranking of importance nor the order in which the tests ~~should~~ shall be performed.

~~NOTE~~ In some cases, it may be necessary to perform production sample tests on complete assemblies in addition to the routine tests, for example when modifications are introduced in the course of production. The nature and extent of such additional tests ~~should~~ shall be agreed on a case-by-case basis.

14.5 Production test objectives

14.5.1 Visual inspection

To check that all materials and components are undamaged and are correctly installed in accordance with the latest approved revision of the production documentation.

14.5.2 Connection check

To check that all the main current-carrying connections have been made correctly.

14.5.3 Voltage-grading circuit check

To check the grading circuit parameters and thereby ensure that voltage division between series-connected levels will be correct for applied voltages from DC to impulse waveshapes, if applicable.

14.5.4 Control, protection and monitoring circuit checks

To check the function of any control, protection or monitoring circuits that form an integral part of the valve, such as IGBT gate drive circuits and any local protection or monitoring circuits.

If type tests and tests of the effectiveness of fuse protection are considered to be necessary, they shall be specified separately with conditions for tests.

14.5.5 Voltage withstand check

To check that the valve components can withstand the voltage corresponding to the maximum value specified for the valve. The checks shall include AC–DC test voltage and switching impulse as applicable.

~~**13.4.6 Partial discharge tests**~~

~~To demonstrate correct manufacture, the purchaser and supplier shall agree which components and subassemblies are critical to the design, and appropriate partial discharge tests shall be performed.~~ **23**

14.5.6 Turn-on / turn-off check

To check that the IGBT(s) in each valve level turns on and turn off correctly in response to switching commands.

14.5.7 Pressure test

To check that there are no coolant leaks.

15 Presentation of type test results

The type test report shall be issued in accordance with the general guidelines as given in ISO/IEC 17025, and shall include the following information:

– name and address of the laboratory and location where the tests were carried out;
– name and address of the purchaser;
– unambiguous identification of the test object, including type and ratings, serial number and any other information aimed to identify the test object;
– dates of performance of the tests;
– description of test circuits and test procedures used for the performance of the tests;
– reference to the normative documents and clear description of deviations, if any, from procedures stated in the normative documents;
– description of measuring equipment and statement of the measuring uncertainty;
– test results in the form of tables, graphs, oscillograms, and photographs as appropriate;
– description of equipment or component failure;
– other data/statement/description as intention of evidence in lieu.

Annex A
(informative)

Overview of VSC converters in HVDC power transmission

A.1 General

Voltage sourced converter (VSC) valves are an ~~emerging~~ evolving technology, in which different manufacturers may have substantially different technological approaches and where, in the future, there may be new circuit topologies that have not yet been described.

Voltage sourced converters for HVDC differ fundamentally from conventional HVDC converters (which are ~~current sourced~~ line commutated converters) in that in order to reverse the direction of power flow, it is the direction of direct current, not the polarity of direct voltage, that is reversed. Smoothing of the direct voltage is performed by a large DC capacitor, which plays an analogous role to the DC inductor (which may partly be fulfilled by the inductance of the DC transmission system and the leakage inductance of the converter transformers) in a conventional HVDC project.

In fact, in a great many respects, the role of voltage in a VSC valve is equivalent to that of current in a conventional HVDC thyristor valve, and vice-versa.

A detailed treatment of all possible VSC valve technologies is far beyond the scope of this standard. The purpose of this annex is simply to present a brief overview of the main differences between VSC and conventional HVDC thyristor valves, and of the main types of VSC valve, insofar as they affect the criteria for testing such valves.

This annex is intended to give an overview of the main converter technologies known at the time of writing. However, it is not intended to limit or constrain in any way the types of technology that can be utilized.

For determination and evaluation of the VSC valve losses, information is provided in Annex C.

A.2 VSC basics

All voltage sourced converters aim to synthesize, from the DC capacitor voltage, an approximately sinusoidal voltage at the AC terminals. However, in practice, the output voltage of the VSC cannot be perfectly sinusoidal but instead consists of a number of discrete steps of voltage, or "output levels". The term "level" here refers to a discrete output voltage level and should not be confused with the term "VSC valve level" which refers to a physical building-block of the valve, for example an individual IGBT and associated components.

For power systems, 3-phase converters are almost always used, but in considering the number of output levels of a converter, each "phase unit" of the converter is normally considered independently. The number of output levels refers to the number of discrete states in which the line-to-neutral output voltage of a phase unit can exist (Figure A.1). It is important to note that an n-level converter will have ($2n$-1) possible values of line-to-line voltage.

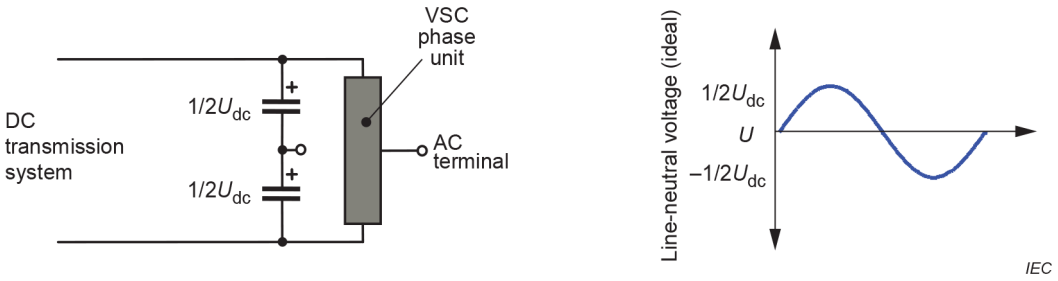
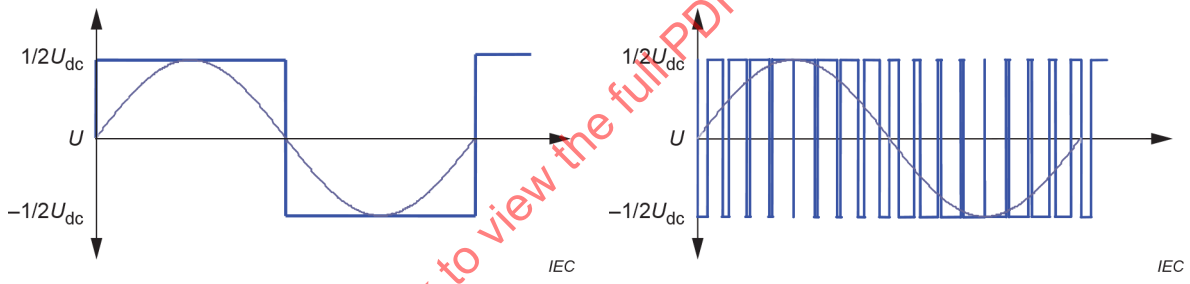


Figure A.1 – A single VSC phase unit and its idealized output voltage

In the simplest possible VSC topology, the "two-level converter", the AC output voltage of each phase arm (with respect to the midpoint of the DC capacitor, which is normally earthed) has only two possible states: $+½U_{dc}$ and $–½U_{dc}$.

If the VSC valves in this phase arm are switched only at fundamental frequency, the resulting AC output voltage waveform is an extremely poor approximation to sinusoidal. Such a waveform would be totally unacceptable in a power system.

However, by switching the valves ON and OFF more than once per fundamental frequency cycle and employing pulse width modulation (PWM) it is possible to obtain an output voltage that is, after filtering, reasonably sinusoidal. Figure A.2 illustrates both cases.



a) Without PWM b) With PWM

Figure A.2 – Output voltage of a VSC phase unit for a 2-level converter

PWM is an established technique in converters for motor drives, but carries the disadvantage of much increased switching losses.

An alternative to PWM is to use a more complex converter with a higher number of output levels – a "multi-level converter". There are a number of 3-level or 5-level converter topologies available, but in a power system application these too will generally still require PWM in order to obtain sufficiently low harmonics.

However, there are some converter topologies that are capable of producing much higher numbers of output levels, such that even without using PWM, the output voltage waveform is highly sinusoidal and little or no filtering is required. Figure A.3 shows the output voltage of a 15-level converter, which can be seen to be reasonably sinusoidal. In practice, higher numbers of levels than 15 would normally be used for HVDC transmission applications.

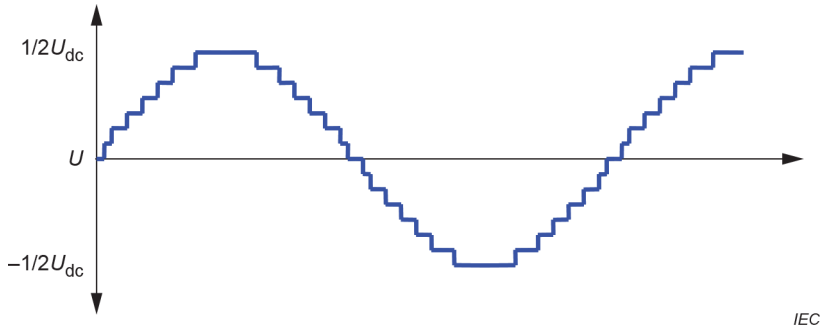


Figure A.3 – Output voltage of a VSC phase unit for a 15-level converter, without PWM

A.3 Overview of main types of VSC valve

Unlike conventional HVDC thyristor valves, which have evolved towards a largely common overall design, VSC valves are at an early stage in their technological evolution and exist in a number of forms.

At the time of writing of this standard, the VSC valves that are available commercially fall into two basic categories.

- Switch type VSC valves. These valves, like their thyristor counterparts, function only as a controllable switch, with only two permanent states: ON and OFF. In converters based on this topology, the DC capacitors are completely separated from the valves and can be tested in isolation.
- Controllable voltage source type VSC valves. In valves of this type, the DC capacitors form an integral part of the valve and cannot conveniently be separated from it for testing purposes.

Certain type tests need to be performed in a quite different way depending on which of the above categories the valve falls into.

Some other categories of "hybrid" VSC valve have also been described in literature and exhibit a mixture of characteristics from the two categories above; however at the time of writing, development work in these topologies is in the relatively early stages and these topologies are not yet commercially available.

A.4 Switch type VSC valve

A.4.1 General

VSC valves of this type bear a close apparent resemblance to conventional thyristor valves, in that they consist of a large number of series connected IGBT devices which are switched simultaneously. As with conventional thyristor valves, simultaneous switching of the series connected IGBTs is vital. Redundancy can be provided in the same way as for an LCC thyristor valve, by providing a few additional IGBT devices in series and either ensuring that the IGBTs are of a special type with short-circuit failure mode or are equipped with a parallel-connected shorting switch.

Valves of this type are normally used with converters with a relatively low number of output levels. To compensate for the low number of output levels, such converters usually use pulse width modulation (PWM) to achieve a good approximation of a sinusoidal output voltage.

Some of the more common converter topologies that can be used with this type of VSC valve are described below.

A.4.2 2-level converter

In this, the simplest type of VSC, each VSC phase unit comprises just two VSC valves connected in series and sharing an AC terminal. The two valves are switched alternately such that, at any given time, either one or the other valve is conducting, but never both. (In practice, there is usually a slight dead-time or "underlap" between the two valves in order to prevent a "shoot-through" or simultaneous conduction of the two valves in series).

The circuit topology of this converter is very simple (see Figure A.4) and requires very little explanation. When V1 is conducting, the AC terminal is connected to the upper DC terminal and therefore produces an output voltage of $+½U_{dc}$. When V2 is conducting, the AC terminal is connected to the lower DC terminal and therefore produces an output voltage of $–½U_{dc}$.

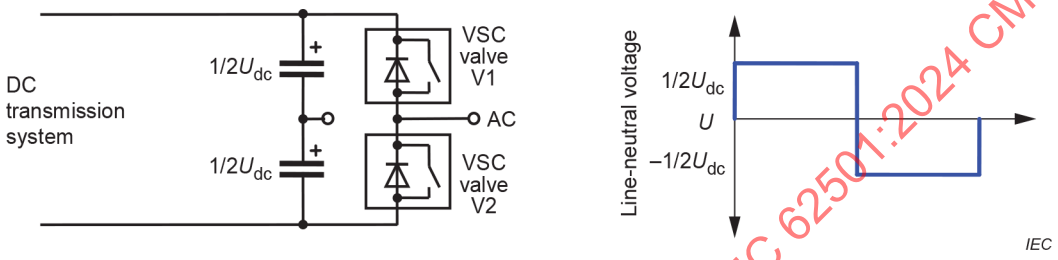


Figure A.4 – Basic circuit topology of one phase unit of a 2-level converter

A.4.3 Multi-level diode clamped converter

In this family of converters, the DC capacitor is sub-divided into a number of discrete stages connected in series, more than two IGBT valves are provided per phase unit and diode valves are used to connect between various intermediate points in the DC capacitor and in the phase unit.

In the simplest version of this circuit (see Figure A.5), the three-level converter, each phase unit contains four independent VSC valves connected in series. The DC capacitor is subdivided into two series-connected units (as it frequently is for a 2-level converter). The AC terminal is connected to the terminal between V2 and V3, and the ¼ and ¾ points (between valves V1/V2 and V3/V4) are connected to the DC midpoint via diode valves.

With this converter, three output states are possible from a single phase unit. When valves V1+V2 are conducting, the AC terminal is connected to the upper DC terminal and therefore produces an output voltage of $+½U_{dc}$. When valves V3+V4 are conducting, the AC terminal is connected to the lower DC terminal and therefore produces an output voltage of $–½U_{dc}$. When valves V2+V3 are conducting, the AC output voltage is "clamped" at the DC midpoint voltage by the diode valves.

The same principle can be extended to higher numbers of levels by further subdividing the DC capacitor and using more VSC and diode valves. In a 5-level converter, the DC capacitor is subdivided into four discrete stages, and there are eight VSC valves and six diode valves (see Figure A.6). In this circuit, the valves are switched in adjacent groups of four, for example V1+V2+V3+V4 gives an output voltage of $+½U_{dc}$, V2+V3+V4+V5 gives an output voltage of $+¼U_{dc}$, etc.

It can be seen that as the number of output levels increases, the complexity of the circuit increases disproportionately. This is made worse by the fact that not only the number, but also the voltage rating of the diode valves increases rapidly with the number of output levels.

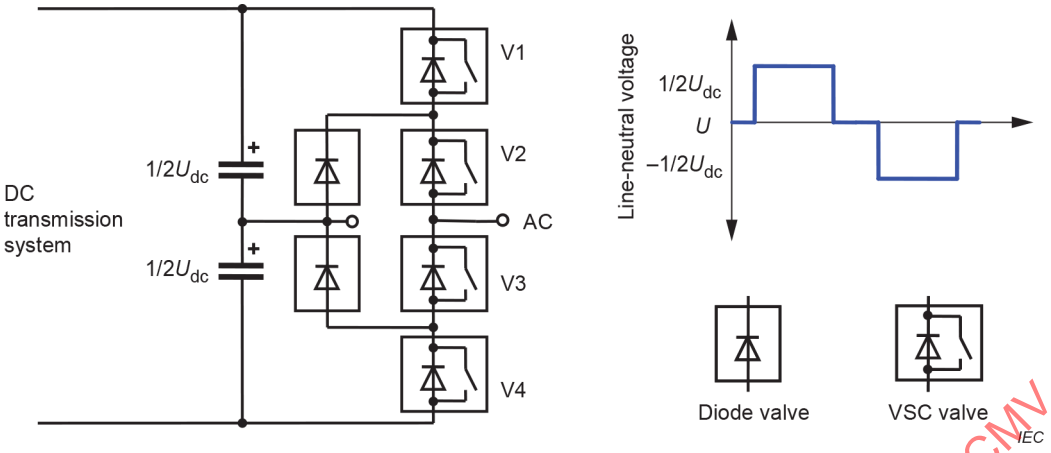


Figure A.5 – Basic circuit topology of one phase unit of a 3-level diode-clamped converter

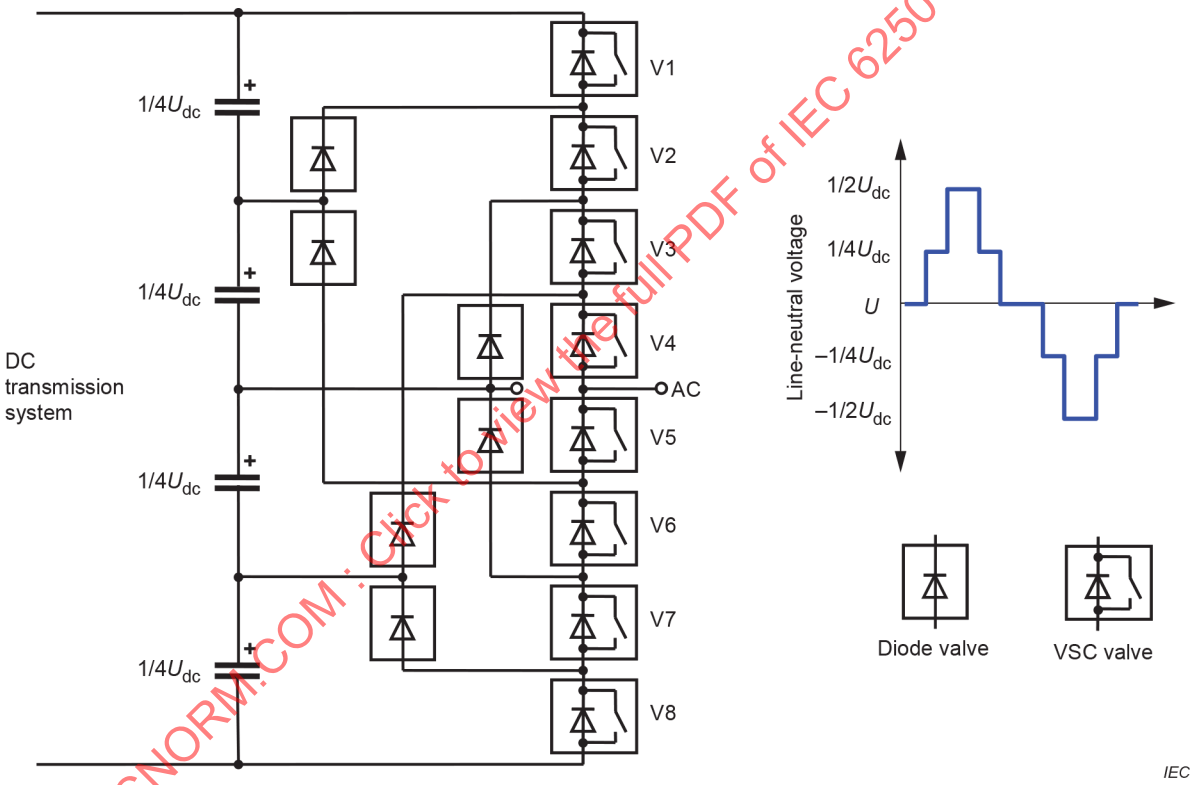


Figure A.6 – Basic circuit topology of one phase unit of a 5-level diode-clamped converter

A.4.4 Multi-level flying capacitor converter

This circuit achieves the same result as the diode-clamped converter by a different method. Instead of using diode valves to clamp the output voltage to one of the intermediate DC capacitor stages, it uses one or more additional DC capacitors, which are isolated from the DC terminals and hence "floating" or "flying", to achieve the same effect. This circuit is sometimes also referred to as the "Foch-Meynard" circuit after its inventors.

The 3-level flying capacitor converter (see Figure A.7) has a single flying capacitor with a nominal voltage of ½U_{dc}. This capacitor is connected between the terminals shared by V1/V2 and those shared by V3/V4. As with the 3-level diode-clamped converter, valves are switched in pairs but the pattern to achieve zero output voltage is different. To achieve an output state of 0, either valves V1+V3 or valves V2+V4 are switched on. V2+V3 is an illegal combination as it would short-circuit the flying capacitor.

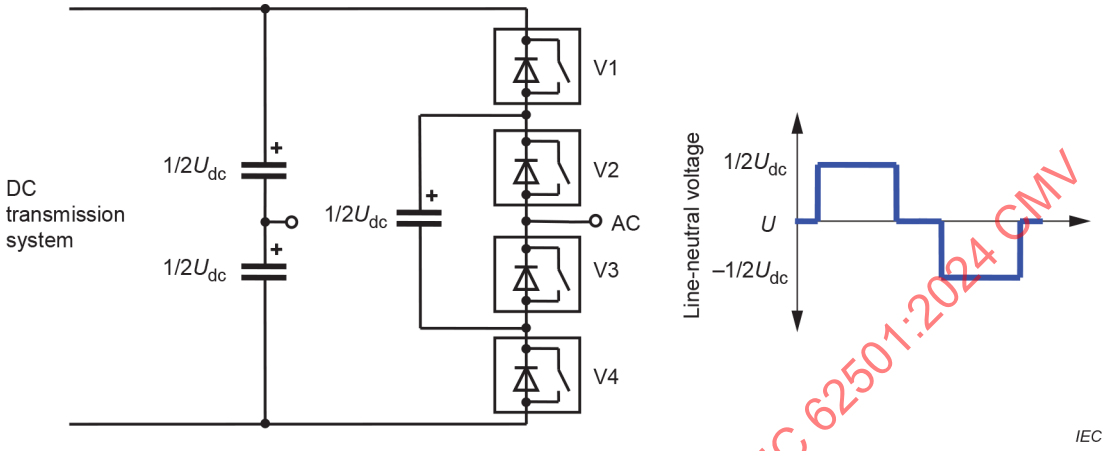


Figure A.7 – Basic circuit topology of one phase unit of a 3-level flying capacitor converter

The number of VSC valves per phase unit is the same for this converter as it is for a diode-clamped converter with the same number of output levels. Like the diode-clamped converter, higher numbers of output levels are possible, but at the expense of disproportionately increased complexity.

A.5 Controllable voltage source type VSC valve

A.5.1 General

In the 2-level converter, the valves and DC capacitor are clearly separated items of equipment and can be designed and tested in isolation. However, as the number of output levels increases, it is seen from Subclauses A.4.3 and A.4.4 that the DC capacitor(s) become increasing subdivided and the valves and DC capacitor become increasingly inter-dependent.

As the converter starts to approach the ideal, where the number of output levels is sufficient to obtain a good approximation to a sinusoidal waveform without using PWM, the subdivision of the DC capacitor and the interconnectivity between capacitors and IGBTs can become so complex that it is no longer practical to make a clear distinction between the two. In such cases, it may be more convenient to consider the "VSC valve" to be not simply the IGBT elements that perform the switching, but also the distributed DC capacitors. In effect, such a valve is no longer simply a switch but is now a controllable voltage source, connected between the AC terminal of the corresponding phase unit, and one of the DC terminals (see Figure A.8).

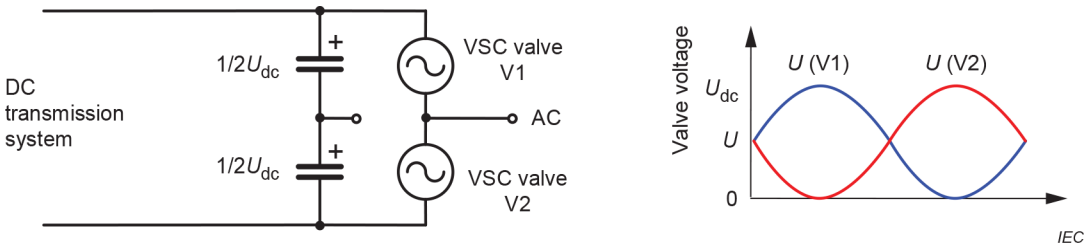


Figure A.8 – A single VSC phase unit with controllable voltage source type VSC valves

Each of the valves V1 and V2 in the phase unit produces an output voltage consisting of a sinusoidal AC component with a DC offset (equal to ½ U_{dc}). The output voltages of the two valves are varied such that at any given time, U(V1) + U(V2) = U_{dc}.

In principle, there can be many different methods of implementing such a valve, but two (closely related) methods have found widespread application: the modular multi-level converter (MMC) and the cascaded two-level converter (CTL).

~~Since the circuit is inherently modular, it is relatively straightforward to obtain high numbers of output levels, without requiring either PWM (which leads to higher switching losses and requires filtering) or series-connected IGBTs (which leads to problems of ensuring voltage distribution). On the other hand, the number and size of discrete d.c. capacitors required can be considerable, and there may be difficulties in ensuring that all d.c. capacitor voltages remain balanced. In comparison with two- or three-level converters, therefore, this topology allows for a simpler valve design and lower losses at the expense of a more complex controls architecture and greater space requirement.~~

A.5.2 Modular multi-level converter (MMC)

One implementation of the MMC circuit is shown in Figure A.9. The circuit of each submodule is modular, each submodule comprising a single, isolated DC capacitor and two IGBT switches. In effect, this circuit is very similar to that of the basic 2-level converter (see Figure A.4) except that the interconnections between submodules are made from the AC terminal (between IGBT1 and IGBT2) of one submodule, to one of the DC terminals of the neighbouring submodule. With this circuit, each submodule can produce two discrete output states: U = 0 (obtained by switching IGBT2 on) or U = $U_{dc\_submodule}$ (obtained by switching IGBT1 on). $U_{dc\_submodule}$ is the DC link voltage of a single submodule, which is much less than U_{dc}, the DC link voltage of the complete system.

With this circuit, it is possible to synthesize a unipolar valve output voltage with a maximum of U = U_{dc} and a minimum of U = 0. However, in common with all the converter topologies discussed so far, the converter has no capacity to suppress the overcurrent which arises from a short-circuit between the DC terminals of the converter. This is because although the two IGBTs can be turned off very quickly, a conducting path always remains through the freewheel diode in parallel with IGBT2.

Another implementation of the MMC circuit addresses this shortcoming by using a full-bridge arrangement, as shown on Figure A.10, instead of the half-bridge arrangement shown in Figure A.9.

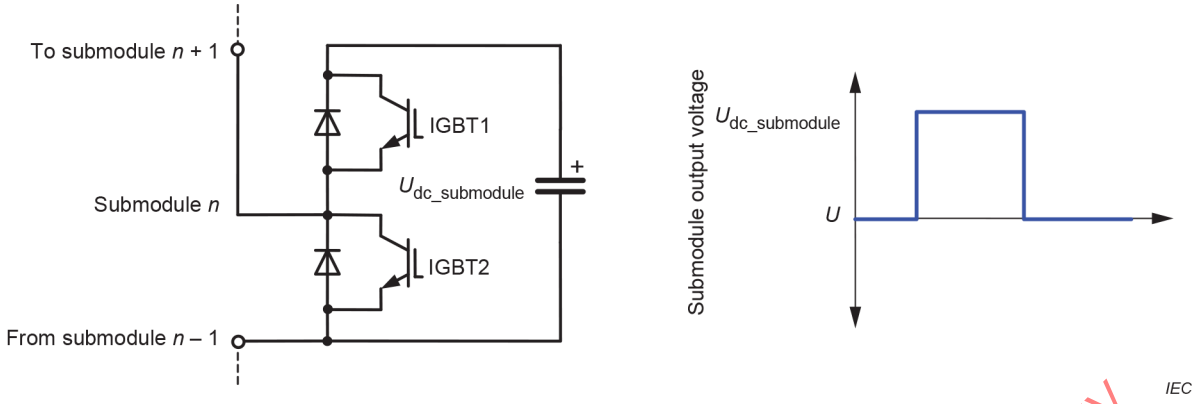


Figure A.9 – The half-bridge MMC circuit

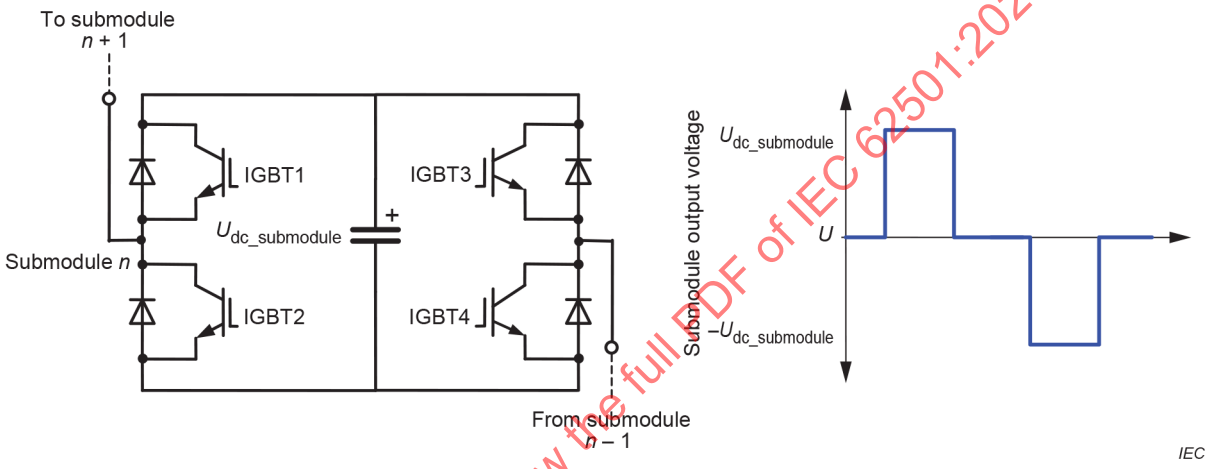


Figure A.10 – The full-bridge MMC circuit

In the full-bridge version of the MMC, each submodule contains four IGBTs instead of two, and can produce three discrete output voltage states:

- U = 0 (obtained by switching on either IGBT1 + IGBT3 or IGBT2 + IGBT4);
- $U = +U_{dc\_submodule}$ (obtained by switching on IGBT1 + IGBT4); or
- $U = -U_{dc\_submodule}$ (obtained by switching on IGBT2 + IGBT3).

The full-bridge circuit allows the valve to synthesize an output voltage of either polarity, allowing a new voltage-sourced converter to be connected as a tap to an existing HVDC line. Even when used on a unipolar DC line, the additional flexibility provided by the circuit allows the AC component of valve voltage to exceed the DC component (which is not possible with the half-bridge circuit), resulting in a lower AC current in the valve. In addition, the ability to suppress fault currents arising from short-circuits between the DC terminals can allow some simplification of protective functions. On the other hand the IGBT component count and the conduction losses, are increased by nearly double compared with the half-bridge version.

Since the MMC circuit is inherently modular, it is relatively straightforward to obtain high numbers of output levels, without requiring either PWM (which leads to higher switching losses and requires filtering) or series connected IGBTs (which leads to problems of ensuring voltage distribution). Industry standard IGBT devices can be used, which is not the case for valves of the switch type. Redundancy cannot be provided within each submodule (because the correct operation of the submodule requires both IGBTs to be healthy) and is usually provided by equipping the valve with a few extra submodules and ensuring that the entire submodule is shorted out in the event of a failure.

On the other hand, the number and size of discrete DC capacitors required can be considerable, and there may be difficulties in ensuring that all DC capacitor voltages remain balanced. In comparison with two- or three-level converters, therefore, this topology allows for a simpler valve design and lower losses at the expense of a more complex controls architecture and greater space requirement.

A.5.3 Cascaded two-level converter (CTL)

An advantage of the MMC circuit is that it avoids the need for IGBTs to be directly connected and switched synchronously in series. However, it is also possible to realise the MMC circuit with more than one IGBT in series in each switching position. Converters designed in this way are referred to as cascaded two-level converters in order to distinguish them from the MMC circuit, although in nearly every respect the circuit functions in exactly the same way as the MMC circuit.

In common with the MMC circuit, the CTL circuit can exist in half-bridge and full-bridge variants. The building-block of the CTL valve is referred to as a "cell" and the half-bridge version of a cell is shown on Figure A.11. Each of the two switch positions consists of n IGBTs in series, switched synchronously, and the cell DC capacitor will operate at approximately n times the voltage of a submodule DC capacitor in the MMC circuit.

In operational terms the only significant difference between the CTL and MMC circuits is that the CTL circuit produces a valve output voltage containing fewer, larger, steps than the MMC circuit. Its harmonic performance is therefore not quite as good as that of the MMC circuit, although if the number of IGBTs per switching position is modest (for example, 5 to 10) then it can still achieve very high waveform quality while permitting some simplification of the control system compared to the MMC circuit. The CTL circuit does, however, require sophisticated IGBT gate drive circuits and a more specialised type of IGBT, in common with all valves of the switch type.

Redundancy is provided within each cell by equipping each switch position with more IGBTs than are normally required to operate within the rated voltage of the converter.

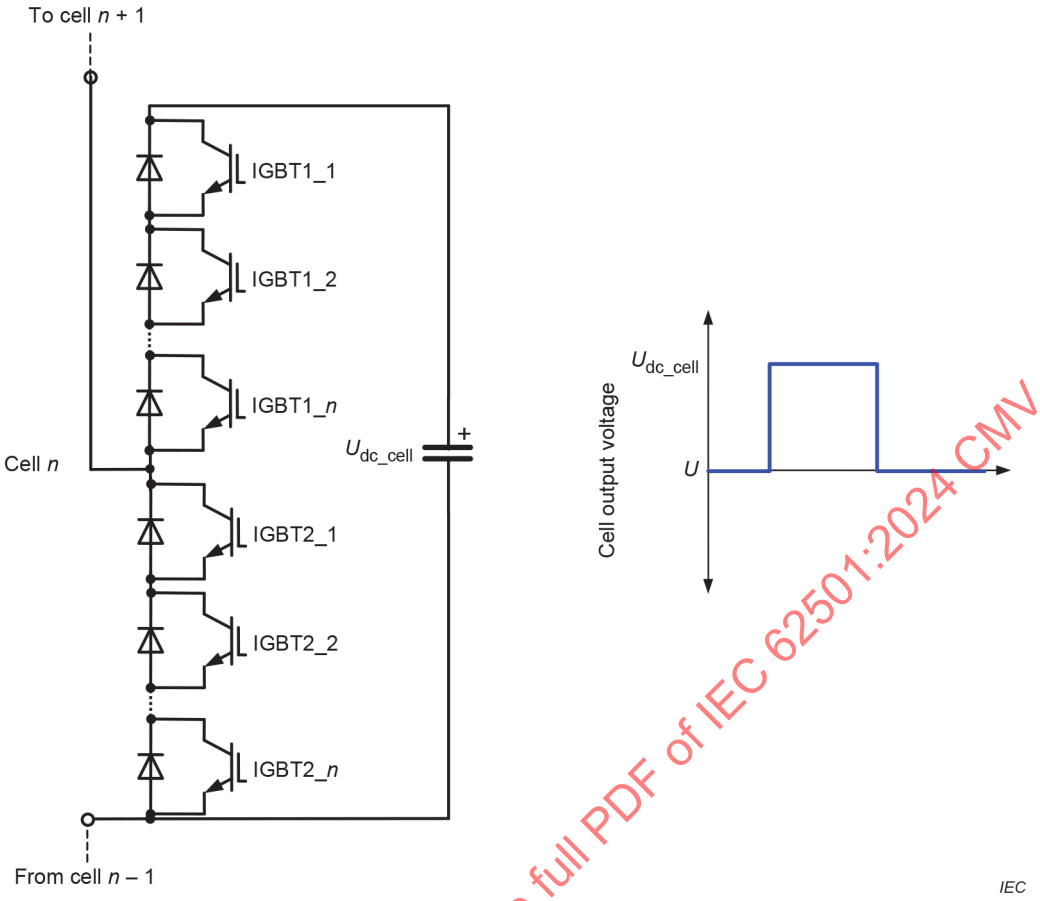


Figure A.11 – The half-bridge CTL circuit

A.5.4 Terminology for valves of the controllable voltage source type

Figure A.12 and Figure A.13 illustrate the main constructional terms for valves of the MMC and CTL type respectively, to explain the meaning of terms such as VSC level, submodule and cell.

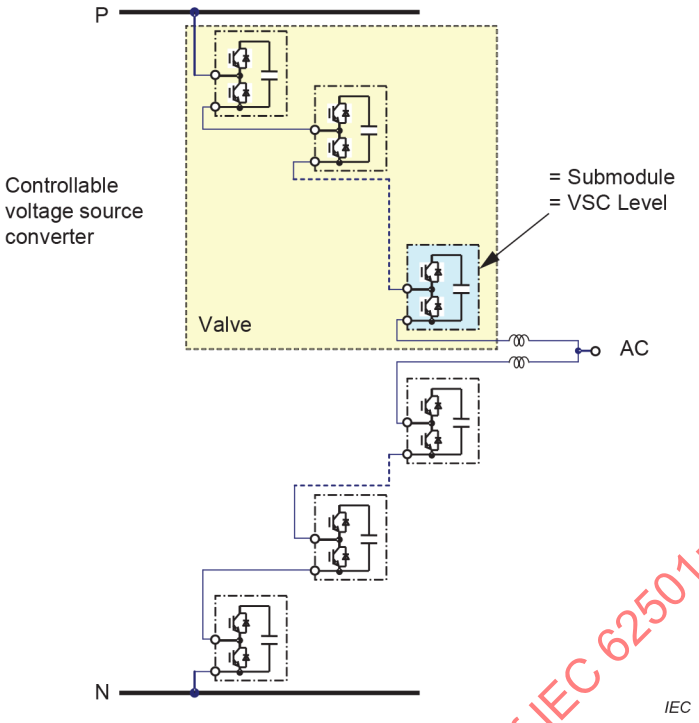


Figure A.12 – Construction terms in MMC valves

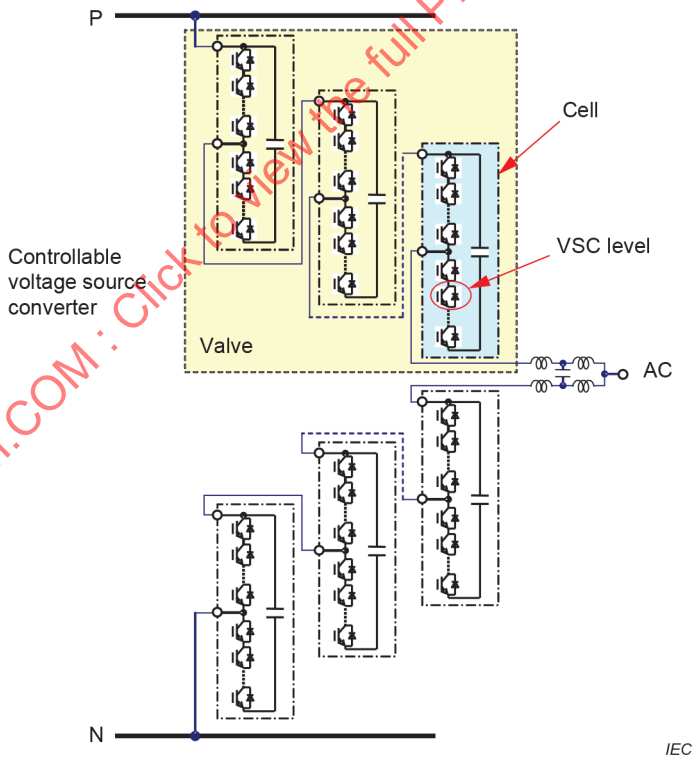


Figure A.13 – Construction terms in CTL valves

A.6 Hybrid VSC valves

Some published literature has suggested alternative types of VSC valve which possess characteristics of both the switch type and controllable voltage source type. Since the pace of development in this field is quite rapid it is considered beyond the scope of this document to present a detailed treatment of these new converter topologies; however, a basic treatment is given in CIGRE Technical Brochure No. 492.

A.7 Main differences between VSC and conventional HVDC valves

VSC valves differ from conventional thyristor-based HVDC valves in many respects. It is important to appreciate these differences in order to understand the differences in approach that need to be taken when testing such valves.

Whilst there are a great many differences, the principal ones that affect valve testing are as follows.

- VSC valves are capable of both being turned ON and being turned OFF by control action. In contrast, conventional HVDC thyristor valves can only be turned ON by control action and, to achieve turn OFF, require the external circuit to force the current to zero and then apply a period of reverse voltage. Hence, tests to demonstrate minimum extinction angles or positive voltage transients during the recovery interval (which are so important for thyristor valves), have no significance for VSC valves.
- In most VSC valves, the valve is not capable of supporting reverse voltage (because it contains in-built freewheel diodes), but can conduct reverse current. In conventional HVDC thyristor valves, the valve can withstand reverse voltage but not conduct reverse current.
- In VSC valves, protective turn-ON is generally not used because of the risk of creating a short-circuit across the DC capacitor, but instead protective turn-OFF is employed as a means of suppressing overcurrents. By contrast, in conventional HVDC thyristor valves, protective turn-ON is widely used and protective turn-OFF is not possible.
- The large DC-side capacitance means that there are few circumstances where a VSC phase unit can experience fast voltage transients between terminals. In valves of the "controllable voltage source" type (where some of the DC capacitance is embedded within the valve) the same is also true for voltages between the terminals of the valve.

Annex B
(informative)

Valve component fault tolerance

Fault tolerance capability may be defined as the ability of an HVDC VSC valve to perform its intended function, until a scheduled shutdown, with faulted components or subsystems or overloaded components, and not lead to any unacceptable failure of other components, or extension of the damage due to the faulted condition. Special features may be required in the design to ensure fault tolerance.

Tests to demonstrate the valve component fault tolerance are not categorized as type tests since most of them are destructive tests of valve or valve components and the tests are usually done on small number of valve levels. Those tests should be done in design stage of new type of valves for compliance check of valve fault component tolerance. Supplier should document the tests and provide project related report, based on experience in lieu, on purchasers' request.

Examples of faults for which fault tolerance may be required are given below: **24**

a) Failure of an IGBT or diode

   Even though a short-circuit IGBT-diode pair or the operation of an external valve level shorting device will shunt the other components at the valve level, in some designs there may be a danger of overload of current connections or changes in clamping load.

b) Missing of on-gate at one valve level due to loss of normal on-gate pulses to that level

   Missing of on-gate leads to parallel overvoltage of the components at the affected level.

c) Insulation failure of a snubber capacitor, snubber resistor or other components if applicable

   Insulation failure of any component in parallel with the IGBTs or diodes can attract load current into it, leading to a hazardous condition.

d) Leakage of small quantities of valve coolant

   If the valve is liquid cooled, small leaks may not be easily detected. Escaped coolant can contaminate sensitive components, leading to malfunction, and can increase the probability of insulation failure. However, experience acquired in the wet test performed on both LCC and VSC valves indicates that the valve wet test on a new and dust free valve surface is unable to identify locations where might cause valve dielectric failure in service due to the leakage of small quantities of valve coolant. IEEE Std 857™-1996, *IEEE Recommended Practice for Test Procedures for High-Voltage Direct-Current Thyristor Valves*, to which the wet test is often referred, was withdrawn in 2010. **25**

e) Submodule / Cell internal short-circuit current

   Either misfiring of IGBT, short-circuit of IGBT-diode pair or insulation failure may lead to an internal capacitor discharge current. Under these short-circuit conditions, the ~~cell shall~~ fault should be self-contained without impacting the normal operation of adjacent submodule / cell. In particular, the fault should not lead to a flashover outside the affected submodule / cell, damage leading to mal-operation caused by projected debris or electromagnetic interference on neighbouring submodule / cell. Any visible light escaping from the faulted submodule / cell should not cause fire or arc detection systems in the valve hall to shut down the converter.

f) Submodule / Cell external short-circuit current

Similarly to case (e) above, if a short-circuit takes place between the external terminals of the submodule / cell, or across several submodule / cell (for example between tiers of a valve stack) then the capacitors of the submodule / cell(s) that were in the output state at the time of the short circuit, will discharge their capacitors into the short-circuit. Although the rate of change of current is lower than for case (e) because of the larger loop inductance, it is still very high and can lead to a severe rate of change of magnetic field, potentially affecting nearby electronic circuits. Depending on the design philosophy adopted for the valve, tests may be needed to demonstrate that the IGBTs will safely turn off before the capacitors can fully discharge and that the resulting electromagnetic disturbance does not cause mal-operation of nearby electronic circuits.

g) Effects of fast transient overvoltages on electronics

Certain events such as lightning strikes on the AC or DC systems close to the converter station, switching actions of the valves (including protective blocking) and bushing flashovers inside the valve hall may lead to fast transient overvoltages which, although not necessarily of an amplitude sufficient to pose a risk of insulation failure, could subject the electronic boards in the valve to a very high dv/dt. Depending on the design philosophy of the overall converter station for such faults, tests may be necessary to demonstrate that the electronic boards continue in operation without damage or malfunction under such conditions.

The purchaser should review the design offered with the supplier to determine the probability and likely consequences of certain failures. Where appropriate, consideration should be given, to the performance of special tests to verify critical aspects of the fault tolerance capability of the valve. The details of such tests are subject to agreement on a case-by-case basis.

Annex C 26
(informative)

Valve losses determination

As transmission losses are directly related to the investment and operational costs, they are one of the most important factors for high voltage direct current (HVDC) project evaluation. For voltage sourced converters (VSC), valve losses are the largest part of the total converter station losses and therefore the determination and evaluation of the VSC valve losses becomes highly important.

Presently, the losses of VSC valves are determined based on the calculation methods of IEC 62751-1 and IEC 62571-2. The calculation method requires detailed information such as the parameters of semiconductor devices, VSC valve design characteristics and operating modes, which are usually not directly available to the HVDC system purchaser/user, who consequently finds it difficult to evaluate the calculated losses results.

Therefore, CIGRE working group B4.75 was set up in 2017 to perform a feasibility study to assess laboratory loss measurement methods on VSC valves for loss calculation evaluation purposes and to make recommendations considering the pros and cons of such measurement methods versus the methods in IEC 62751. The results of this working group were published in 2021 as CIGRE TB 844: "Feasibility study for assessment of lab losses measurement of VSC valves".

The brochure starts with a general description of losses in VSC HVDC converter valves, the origins of different losses in components, the dependency of the losses on different operating modes, as well as special aspects of different designs. This is followed by a summary of the current practice for valve losses determination, including the modelling of the semiconductor parameters and then by a discussion on how the transparency of the overall calculation process can be enhanced. As the main study results of the WG B4.75, an evaluation of the existing methods to measure losses is provided. This is complemented by an overview of the operation conditions and additional aspects for losses measurement (such as commercial aspects) that need to be taken into account. In the last part, the results are summarized and recommendations for application of losses measurement are given, which can be used as guidance for the introduction of losses measurements in the operational type tests of VSC valves.

The conclusion of CIGRE TB 844 is that the laboratory measurement of valve losses is feasible, although the level of accuracy achievable is still quite poor. The general recommendation therefore is that the laboratory measurement should become a standard part of the operational type tests of the VSC valves, such that in the coming years greater industry experience can be gained in this area. However, it is not recommended that the measured valve losses are used as part of the financial evaluation criteria for the HVDC project, until there is a good industry experience and consensus over what should be a realistically achievable level of measurement uncertainty.

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IEC 61975, *High-voltage direct current (HVDC) installations – System tests*

IEC TR 62543, *High-voltage direct current (HVDC) power transmission using voltage sourced converters (VSC)*

IEC 62751-1, *Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems – Part 1: General requirements*

IEEE Std 857™-1996, *IEEE Recommended Practice for Test Procedures for High-Voltage Direct-Current Thyristor Valves*

CIGRE Technical Brochure No. 269, *VSC Transmission*

CIGRE Technical Brochure No. 447, *Components Testing of VSC Systems for HVDC Applications*

CIGRE Technical Brochure No. 492, *Voltage Sourced Converter (VSC) for HVDC Power Transmission – Economic Aspects and Comparison with other AC and DC Technologies*

CIGRE Technical Brochure No. 844, *Feasibility study for assessment of lab losses measurement of VSC valves*

List of comments

1 System requirements and operation conditions for VSC valves used in energy storage systems (ESS) are the same or similar to those requirements for VSC valves used in HVDC power transmission systems.

2 Check-list and criteria added to support the use of evidence in lieu.

3 For VSC valves, each type test is essentially independent of, and does not influence, the other type tests.

4 Extension of the valve position fault table by a further line. An independent continuation of the table no longer appears necessary, as such converter sizes do not appear plausible.

5 Differentiation of the AC-DC voltage test into two different process methodologies (for further information see Subclause 9.4.1 or Subclause 9.4.2).

6 Added appropriate test voltage definition for controllable VSC type valves. Here, voltage per valve level is relevant (not along entire valve).

7 Further clarification and harmonized with IEC 62927.

8 More text added to show further possibilities and variants.

9 Clarify the definition and avoid possible mis-use in valve test when HVDC system has an action of fast discharge devices or re-configuration at fault.

10 Test factor for the long period has been increased to harmonize it with DC voltage test.

11 Guide added for application with a site altitude above 1 000 m. More information is available in IEC 60700-1, Annex A.

12 Corresponding to the changes introduced in Subclause 9.4.3.1. In valve AC-DC voltage test the valve electronics is energized when test voltage is applied.

13 More text added to support the readers to understand the difference between VSC valves and other high-voltage test objects. Commonly used dielectric test methods used in test of other high voltage equipment, for examples: thyristor valves for HVDC converters, thyristor valves for FACTS applications, …, are not applicable.

14 Has to be used in order to acquire a credible result.

15 More text added to describe how to use Method 2 in test.

16 Differentiation of the AC-DC voltage test into two different procedure methodologies dependent on the converter structure technology (for further information see explicitly Subclause 9.4.1 or Subclause 9.4.2).

17 Changes introduced below are editorial changes only for easy understanding.

18 Alternative tests introduced to make the test done in a convenient way.

19 More information added in the NOTES below on possible valve impulses in operation.

20 Valve levels in controllable voltage source type VSC valves are switched on and off independently with no need for synchronous control. There is no voltage sharing issue after IGBT turn-off.

21 More text added to guide the actual laboratory test.

22 Valve electronics are not involved in entire short-circuit current period in some VSC valve designs. Energization of the valve electronics is therefore meaningless in test of those valves.

23 Partial discharge tests cannot be done with the presence of valve electronics and submodule capacitor. Multiple dis-assembling and re-assembling actions needed in this test which are not in support of product quality control. Deletion of this test item leads this publication harmonized with IEC 62927.

24 One more possible fault and effects of fast transient overvoltage on valve power electronics added as f) and g).

25 More info added.

26 New information part added to present the status of valve losses determination.

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IEC 62501

Edition 2.0 2024-04

INTERNATIONAL STANDARD

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Voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission – Electrical testing

Valves à convertisseur de source de tension (VSC) pour le transport d'énergie en courant continu à haute tension (CCHT) – Essais électriques

IEC 62501:2024-04(en-fr)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) POWER TRANSMISSION – ELECTRICAL TESTING

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IEC 62501 has been prepared by subcommittee 22F: Power electronics for electrical transmission and distribution systems, of IEC technical committee 22: Power electronic systems and equipment. It is an International Standard.

This second edition cancels and replaces the first edition published in 2009, Amendment 1:2014 and Amendment 2:2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) Conditions for use of evidence in lieu are inserted as a new Table 1;
b) Test parameters for valve support DC voltage test, 7.3.2, and MVU DC voltage test, 8.4.1, updated;
c) AC-DC voltage test between valve terminals, Clause 9, is restructured and alternative tests, by individual AC and DC voltage tests, added in 9.4.2;

d) Partial discharge test in routine test program is removed;

e) More information on valve component fault tolerance, Annex B, is added;

f) Valve losses determination is added as Annex C.

The text of this International Standard is based on the following documents:

Draft	Report on voting
22F/731/CDV	22F/748A/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

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VOLTAGE SOURCED CONVERTER (VSC) VALVES FOR HIGH-VOLTAGE DIRECT CURRENT (HVDC) POWER TRANSMISSION – ELECTRICAL TESTING

1 Scope

This International Standard applies to self-commutated converter valves, for use in a three-phase bridge voltage sourced converter (VSC) for high voltage DC power transmission or as part of a back-to-back link, and to dynamic braking valves. It is restricted to electrical type and production tests.

This document can be used as a guide for testing of high-voltage VSC valves used in energy storage systems (ESS).

The tests specified in this document are based on air insulated valves. The test requirements and acceptance criteria can be used for guidance to specify the electrical type and production tests of other types of valves.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060 (all parts), *High-voltage test techniques*

IEC 60071 (all parts), *Insulation co-ordination*

IEC 60270, *High-voltage test techniques – Partial discharge measurements*

IEC 60700-1:2015, *Thyristor valves for high voltage direct current (HVDC) power transmission – Part 1: Electrical testing*
IEC 60700-1:2015/AMD1:2021

IEC 62747, *Terminology for voltage-sourced converters (VSC) for high-voltage direct current (HVDC) systems*

ISO/IEC 17025, *General requirements for the competence of testing and calibration laboratories*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62747 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1 Insulation coordination terms

3.1.1
test withstand voltage
value of a test voltage of standard waveshape at which a new valve, with unimpaired integrity, does not show any disruptive discharge and meets all other acceptance criteria specified for the particular test, when subjected to a specified number of applications or a specified duration of the test voltage, under specified conditions

3.1.2
internal insulation
air external to the components and insulating materials of the valve, but contained within the profile of the valve or multiple valve unit

3.1.3
external insulation
air between the external surface of the valve or multiple valve unit and its surroundings

3.2 Power semiconductor terms

3.2.1
turn-off semiconductor device
controllable semiconductor device which may be turned on and off by a control signal, for example an IGBT

Note 1 to entry: There are several types of turn-off semiconductor devices which can be used in VSC converters for HVDC. For convenience, the term IGBT is used throughout this standard to refer to the main turn-off semiconductor device. However, the standard is equally applicable to other types of turn-off semiconductor devices.

3.2.2
insulated gate bipolar transistor IGBT
turn-off semiconductor device with three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C)

Note 1 to entry: By applying appropriate gate to emitter voltages, the load current can be controlled, i.e. turned on and turned off.

3.2.3
free-wheeling diode
FWD
power semiconductor device with diode characteristic

Note 1 to entry: A FWD has two terminals: an anode (A) and a cathode (K). The current through FWDs is in the opposite direction to the IGBT current.

Note 2 to entry: FWDs are characterized by the capability to cope with high rates of decrease of current caused by the switching behaviour of the IGBT.

3.2.4
IGBT-diode pair
arrangement of IGBT and FWD connected in inverse parallel

3.3 Operating states of converter

3.3.1
blocking state
condition of the converter, in which a turn-off signal is applied continuously to all IGBTs of the converter

Note 1 to entry: Typically, the converter is in the blocking state condition after energization.

3.3.2
de-blocked state
condition of the converter, in which turn-on and turn-off signals are applied repetitively to IGBTs of the converter

3.3.3
valve protective blocking
means of protecting the valve or converter from excessive electrical stress by the emergency turn-off of all IGBTs in one or more valves

3.3.4
voltage step level
voltage step caused by switching of a valve or part of a valve during the de-blocked state of the converter

Note 1 to entry: For valves of the controllable voltage source type, the voltage step level corresponds to the change of voltage caused by switching one submodule or cell. For valves of the switch type, the voltage step level corresponds to the change of voltage caused by switching the complete valve.

Note 2 to entry: Annex A gives an overview of VSC converters in HVDC power transmission.

3.4 VSC construction terms

3.4.1
VSC phase unit
equipment used to connect the two DC busbars to one AC terminal

3.4.2
switch type VSC valve
arrangement of IGBT-diode pairs connected in series and arranged to be switched simultaneously as a single function unit

3.4.3
controllable voltage source type VSC valve
complete controllable voltage source assembly, which is generally connected between one AC terminal and one DC terminal

3.4.4
diode valve
semiconductor valve containing only diodes as the main semiconductor devices, which might be used in some VSC topologies

3.4.5
dynamic braking valve
complete controllable device assembly, which is used to control energy absorption in braking resistor or other components

3.4.6
valve
VSC valve, dynamic braking valve or diode valve according to the context

3.4.7
submodule
part of a VSC valve comprising controllable switches and diodes connected to a half bridge or full bridge arrangement, together with their immediate auxiliaries, storage capacitor, if any, where each controllable switch consists of only one switched valve device connected in series

3.4.8
cell
MMC building block where each switch position consists of more than one IGBT-diode pair connected in series

Note 1 to entry: See Figure A.13.

3.4.9
VSC valve level
smallest indivisible functional unit of VSC valve

Note 1 to entry: For any VSC valve in which IGBTs are connected in series and operated simultaneously, one VSC valve level is one IGBT-diode pair including its auxiliaries (see Figure A.13). For MMC type without IGBT-diode pairs connected in series one valve level is one submodule together with its auxiliaries (see Figure A.12).

3.4.10
diode valve level
part of a diode valve composed of a diode and associated circuits and components, if any

3.4.11
redundant levels
maximum number of series connected VSC valve levels or diode valve levels in a valve that may be short-circuited externally or internally without affecting the safe operation of the valve as demonstrated by type tests, and which if and when exceeded, would require shutdown of the valve to replace the failed levels or acceptance of increased risk of failures

Note 1 to entry: In valve designs such as the cascaded two level converter, which contain two or more conduction paths within each cell and have series-connected VSC valve levels in each path, redundant levels shall be counted only in one conduction path in each cell.

3.4.12
dynamic braking valve level
part of a dynamic braking valve comprising a controllable switch and an associated diode, or controllable switches and diodes connected in parallel, or controllable switches and diodes connected to a bridge arrangement, together with their immediate auxiliaries, storage capacitor and energy dissipation resistors, if any

3.5 Valve structure terms

3.5.1
valve structure
structural components of a valve, required in order to physically support the valve modules

3.5.2
valve support
that part of the valve which mechanically supports and electrically insulates the active part of the valve from earth

3.5.3
multiple valve unit
MVU
mechanical arrangement of 2 or more valves or 1 or more VSC phase units sharing a common valve support

Note 1 to entry: A MVU might not exist in all topologies and physical arrangement of converters.

3.5.4
valve section
electrical assembly defined for test purposes, comprising a number of valve levels and other components, which exhibits pro-rated electrical properties of a complete valve

Note 1 to entry: For valves of controllable voltage source type the valve section shall include cell or submodule DC capacitor in addition to VSC valve levels.

Note 2 to entry: The minimum number of VSC or diode valve levels allowed in a valve section is defined along with the requirements of each test.

4 General requirements

4.1 Guidelines for the performance of type tests

4.1.1 Evidence in lieu

Each design of valve shall be subjected to the type tests specified in this document. If the valve is demonstrably similar to one previously tested, the supplier may, in lieu of performing a type test or individual parts of it, submit a test report of a previous type test for consideration by the purchaser. This should be accompanied by a separate report detailing the differences in the design and demonstrating how the referenced type test satisfies the test objectives for the proposed design. Conditions for use of evidence in lieu are listed in Table 1.

Table 1 – Conditions for use of evidence in lieu from another HVDC project

Type test	Clause	Conditions
Operational tests	6	• Equal or smaller number of valve levels to be tested • Same valve level design • Same valve electronics design • Identical or lower voltage stress and thermal stress[a] on each valve level
Dielectric tests on valve support structure	7	• Identical valve structure, including cooling pipes, cable paths, earthing system, if any • Same valve material and geometrical dimension • Equal or higher air clearance to valve hall and other related equipment inside the valve hall • Equal or lower voltage stress, including DC voltage stress, AC voltage stress and impulse voltage stresses
Dielectric tests on multiple valve unit	8	• Same MVU geometry between valves
Dielectric tests between valve terminals	9	• Identical valve structure, including cooling pipes, cable paths and earthing system, if any • Same valve material and geometrical dimension • Equal or lower voltage stress
IGBT overcurrent turn-off test	10	• Same valve level design • Same valve electronics design • Identical or lower prospective current stress
Short-circuit current test	11	• Same valve level design • Same short-circuit bypass components, if any, and function • Same valve electronics design • Identical or lower short-circuit current stress
Tests for valve insensitivity to electromagnetic disturbance	12	• Same as those indicated for Clauses 6 and 9

[a] Semiconductor devices thermal stress is a combined effect of current and cooling. Device thermal stress is characterised by the device junction temperature.

4.1.2 Selection of test object

This subclause does not apply to tests on the valve supporting structure and multiple valve unit. The test object for those tests is defined in 7.2 and 8.3.

a) Type tests may be performed either on a complete valve or MVU, or parts thereof, as indicated in Table 4.

b) The minimum number of valve levels to be operational type tested, depending on the valve levels in a single valve, is as shown in Table 2. This number applies to the type tests in Clauses 6, 10, 11 and 12. Those valve levels shall be tested in one test setup or multiple setups on several valve sections as defined in those clauses.

Table 2 – Minimum number of valve levels to be operational type tested as a function of the number of valve levels per valve

Number of valve levels, including redundant level per valve	Total number of valve levels to be tested
1 to 50	Number of valve levels in one valve
51 to 250	50
≥ 251	20 %

The minimum number of valve levels to be dielectric type tested can be equal to or lower than the number specified for the operational type test.

The minimum number of valve levels, however, shall be representative of the valve dielectric design.

c) Generally, the same valve sections are recommended to be used for all type tests. However, different tests may be performed on different valve sections in parallel, in order to speed up the programme for executing the tests.

d) Prior to commencement of type tests, the valve, valve sections and/or the components of them shall be demonstrated to have withstood the production tests to ensure proper manufacture.

4.1.3 Test procedure

The tests shall be performed in accordance with IEC 60060, where applicable with due account for IEC 60071 (all parts). Partial discharge measurements shall be performed in accordance with IEC 60270.

4.1.4 Ambient temperature for testing

The tests shall be performed at the prevailing ambient temperature of the test facility, unless otherwise specified.

4.1.5 Frequency for testing

AC dielectric tests can be performed at either 50 Hz or 60 Hz. Operational tests shall be performed at the service frequency.

4.1.6 Test reports

At the completion of the type tests, the supplier shall provide type test reports in accordance with Clause 15.

4.1.7 Conditions to be considered in determination of type test parameters

Type test parameters shall be determined based on the worst operating and fault conditions to which the valve can be subjected, according to system studies. Guidance on the conditions can be found in CIGRE Technical Brochure No. 447.

4.2 Atmospheric correction factor

When specified in the relevant clause, atmospheric correction shall be applied to the test voltages in accordance with IEC 60060-1. The reference conditions to which correction shall be made are the following:

– pressure:

- If the insulation coordination of the tested part of the valve is based on standard rated withstand voltages according to IEC 60071-1, correction factors are only applied for altitudes exceeding 1 000 m. Hence if the altitude of the site a_s at which the equipment will be installed is ≤1 000 m, then the standard atmospheric air pressure (b_0 = 101,3 kPa) shall be used with no correction for altitude. If a_s >1 000 m, then the standard procedure according to IEC 60060-1 is used except that the reference atmospheric pressure b_0 is replaced by the atmospheric pressure corresponding to an altitude of 1 000 m ($b_{1\ 000\ m}$).
- If the insulation coordination of the tested part of the valve is not based on standard rated withstand voltages according to IEC 60071-1, then the standard procedure according to IEC 60060-1 is used with the reference atmospheric pressure b_0 (b_0 = 101,3 kPa).

– temperature: design maximum valve hall air temperature (°C);

– humidity: design minimum valve hall absolute humidity (g/m^3).

Realistic worst-case combinations of temperature and humidity which can occur in practice shall be used for atmospheric correction.

The values to be used shall be specified by the supplier.

4.3 Treatment of redundancy

4.3.1 Operational tests

For operational tests, redundant valve levels shall not be short-circuited. The test voltages used shall be adjusted by means of a scaling factor k_n:

$$k_n = \frac{N_{tut}}{N_t - N_r}$$

where

N_{tut} is the number of series valve levels in the test object;

N_t is the total number of series valve levels in the valve;

N_r is the total number of redundant series valve levels in the valve.

4.3.2 Dielectric tests

For all dielectric tests between valve terminals, the redundant valve levels shall be short-circuited. The location of valve levels to be short-circuited shall be agreed by the purchaser and supplier.

NOTE Depending on the design, limitations might be imposed upon the distribution of short-circuited valve levels. For example, there might be an upper limit to the number of short-circuited valve levels in one valve section.

For all dielectric tests on valve section, the test voltages used shall be adjusted by means of a scaling factor k_0:

$$k_0 = \frac{N_{tu}}{N_t - N_r}$$

where

N_{tu} is the number of series valve levels not short circuit connected in the test object;

N_t is the total number of series valve levels in the valve;

N_r is the total number of redundant series valve levels in the valve.

4.4 Criteria for successful type testing

4.4.1 General

Experience in semiconductor application shows that, even with the most careful design of valves, it is not possible to avoid occasional random failures of valve level components during service operation. Even though these failures may be stress-related, they are considered random to the extent that the cause of failure or the relationship between failure rate and stress cannot be predicted or is not amenable to precise quantitative definition. Type tests subject valves or valve sections, within a short time, to multiple stresses that generally correspond to the worst stresses that can be experienced by the equipment not more than a few times during the life of the valve. Considering the above, the criteria for successful type testing set out below therefore permit a small number of valve levels to fail during type testing, providing that the failures are rare and do not show any pattern that is indicative of inadequate design and providing that the failed valve level permits the rest of the valve or valve section to continue operating without degraded performance.

4.4.2 Criteria applicable to valve levels

Criteria applicable to valve levels are as follows.

a) If, following a type test as listed in Clause 5, more than one valve level (alternatively more than 1 % of the tested valve levels, if greater) has become short or open circuited, then the valve shall be deemed to have failed the type tests.

b) If, following a type test, one valve level (or more if still within the 1 % limit) has become short or open circuited, then the failed level(s) shall be restored and this type test repeated.

c) If the cumulative number of short or open circuited valve levels during all type tests is more than 3 % of the tested valve levels, then the valve shall be deemed to have failed the type test.

d) The valve or valve sections shall be checked after each type test to determine whether or not any valve levels have become short or open circuited. Failed IGBT/diode or auxiliary components found during or at the end of a type test may be replaced before further testing.

e) At the completion of the test programme, the valve or valve sections shall undergo a series of check tests, which shall include as a minimum:
   - check for voltage withstand of valve levels;
   - check of the gating circuits;
   - check of the monitoring circuits;
   - check of any protection circuits forming an integral part of the valve;
   - check of the voltage grading circuits.

f) Valve levels short circuits occurring during the check tests shall be counted as part of the criteria for acceptance defined above. In addition to short or open circuited levels, the total number of valve levels exhibiting faults which do not result in valve level short circuit, which are discovered during the type test programme and the subsequent check test, shall not exceed 3 % of the number of tested valve levels in dielectric and operational type tests. If the number of such levels exceeds 3 %, then the nature of the faults and their cause shall be reviewed and additional action, if any, agreed between purchaser and supplier.

g) When applying the percentage criteria to determine the permitted maximum number of short or open circuited valve levels and the permitted maximum number of levels with faults which have not resulted in a valve level becoming short or open circuited, it is usual practice to round off all fractions to the next highest integer, as illustrated in Table 3.

Table 3 – Valve level faults permitted during type tests

Number of valve levels tested	Number of valve levels permitted to become short or open circuited in any one type test	Total number of valve levels permitted to become short or open circuited in all type tests	Additional number of valve levels, in all type tests, which have experienced a fault but have not become short or open circuited
Up to 33	1	1	1
34 to 67	1	2	2
68 to 100	1	3	3
101 to 133	2	4	4

The distribution of short or open circuited levels and of other valve level faults at the end of all type tests shall be essentially random and not show any pattern that may be indicative of inadequate design.

4.4.3 Criteria applicable to the valve as a whole

Breakdown of or external flashover across common electrical equipment associated with more than one valve level of the valve, or disruptive discharge in dielectric material forming part of the valve structure, cooling ducts, light guides or other insulating parts of the pulse transmission and distribution system shall not be permitted.

Component and conductor surface temperatures, together with associated current-carrying joints and connections, and the temperature of adjacent mounting surfaces shall at all times remain within limits permitted by the design.

5 List of type tests

Table 4 lists the type tests given in Clauses 6, 7, 8, 9, 10, 11 and 12.

Table 4 – List of type tests

Type test	Clause or subclause	Test object
Maximum continuous operating duty test	6.4	Valve or valve section
Maximum temporary over-load operating duty test	6.5	Valve or valve section
Minimum DC voltage test	6.6	Valve or valve section
Valve support DC voltage test	7.3.2	Valve support
Valve support AC voltage test	7.3.3	Valve support
Valve support switching impulse test	7.3.4	Valve support
Valve support lightning impulse test	7.3.5	Valve support
MVU DC voltage test to earth	8.4.1	MVU
MVU AC voltage test	8.4.2	MVU
MVU switching impulse test	8.4.3	MVU
MVU lightning impulse test	8.4.4	MVU
Valve AC – DC voltage test	9.4.1 or 9.4.2	Valve or valve section
Valve switching impulse test	9.4.3.2	
Valve lightning impulse test	9.4.3.3	
IGBT overcurrent turn-off test	10	Valve or valve section
Short-circuit current test	11	Valve or valve section
Test for valve insensitivity to electromagnetic disturbance	12	Valve or valve section
NOTE Valve section used in the valve AC–DC voltage test (9.4.1 or 9.4.2), valve switching impulse voltage test (9.4.3.2) and valve lightning impulse voltage test (9.4.3.3) should be a single structure representative of valve dielectric design.		

6 Operational tests

6.1 Purpose of tests

The principal objectives of the operational tests are:

a) to check the adequacy of the VSC/diode level and associated electrical circuits in a valve with regard to current, voltage and temperature stresses in the conducting state, at turn-on and turn-off under the worst repetitive stress conditions;

b) to demonstrate correct interaction between valve electronics and power circuits of the VSC valves.

6.2 Test object

The tests may be performed on either the complete valve or on valve sections. The choice depends mainly upon the valve design and the test facilities available. The tests specified in this clause are valid for valve sections containing five or more series-connected valve levels. If tests with fewer than five levels are proposed, additional test safety factors shall be agreed. Under no circumstances shall the number of series-connected levels for tests be less than three.

The valve or valve sections under test shall be assembled with all auxiliary components. For the valves with valve surge arrester, a proportionally scaled valve arrester may be included.

The coolant shall be in a condition representative of service conditions. Flow and temperature, in particular, shall be set to the most unfavourable values appropriate to the test in question, such that the relevant component temperature(s) are equal to the values applicable in service.

6.3 Test circuit

For valve designs which act as a controllable voltage source and contain in-built DC capacitance, the DC capacitance and its connections to the semiconductor devices are an integral part of the test object.

However, for valve designs which function as switches, where the DC capacitor is separate from the valve, the DC capacitor needs to be correctly represented in the test circuit. In particular, the series stray inductance in the connections between the DC capacitor and the valve, and the stray capacitance across the valve section, shall be correctly reproduced and scaled to the size of valve section under test. Test circuit interconnections shall be of a type that is representative of the type used in the converter, in order not to introduce unrealistic levels of damping due to skin effects.

6.4 Maximum continuous operating duty test

The test needs to reproduce the following parameters based on the worst in service operating conditions of the converter. More than one test may be necessary to reproduce all parameters at their maximum values.

For VSC valves:

- maximum steady-state IGBT junction temperatures;
- maximum steady-state FWD junction temperatures;
- where snubbers are used, maximum steady-state snubber component temperatures;
- maximum steady-state turn-on and turn-off voltage and current.

For diode valves:

- maximum steady-state diode junction temperature;
- where snubbers are used, maximum steady-state snubber component temperatures;
- maximum steady-state diode turn-off voltage and current.

All of these parameters need to be reproduced during the maximum continuous operating duty test. They may be reproduced either in separate tests or as a combined test.

The test voltage shall be based on the maximum continuous direct voltage, the test switching frequency shall be based on the maximum continuous switching frequency and the modulation pattern shall be representative of that used in service.

The test current, in RMS, shall be determined taking harmonic currents into account and any other additional currents through the valve.

The test current value shall incorporate a test safety factor of 1,05.

For switch type valve, the test voltage U_{tpv1} corresponding to the maximum continuous operating DC voltage shall be determined as follows:

$$U_{\text{tpv1}} = U_{\text{dmax}} \times k_{\text{n}} \times k_1$$

where

U_{dmax} is the maximum continuous operating DC voltage of the valve, including ripple;

k_{n} is a test scaling factor according to 4.3.1;

k_1 is a test safety factor;

k_1 = 1,05.

For controllable voltage source type valve the test voltage, U_{tpvl1}, per valve level shall be determined as follows:

$$U_{tpvl1} = U_{cmax} \times k_1$$

where

U_{cmax} is the maximum continuous operating DC voltage of the valve level, including ripple;

k_1 is a test safety factor;

k_1 = 1,05.

The duration of the test shall be not less than 30 min after the exit coolant temperature has stabilized.

6.5 Maximum temporary over-load operating duty test

If the valve is specified for temporary over-load operation, a maximum temporary operating duty test shall be performed.

NOTE Capability of converter valves in a maximum temporary over-load operation is typically in a few seconds of time while valve cooling is unable to act.

The test conditions, where required, shall be determined using the same methodology as in 6.4 above. However, the test current shall be the specified over-load current without a test safety factor.

Prior to the test, the valve or valve section shall be brought to thermal equilibrium under the conditions of 6.4. The temporary operating duty test is then started from this initial condition and continued for a duration equal to the duration of the temporary overload multiplied by 1,2.

After the temporary over-load operation, return to the conditions of maximum continuous operation as in 6.4 and maintain constant for 10 min.

6.6 Minimum DC voltage test

This test is to verify the correct performance of those valve designs in which energy for the valve electronic circuits is extracted from the voltage appearing between the valve terminals.

The test consists of applying a DC voltage between the terminals of the valve or valve section. For this test, only the voltage, not the current, is important.

The correct operation of the valve electronic circuits may be demonstrated either by deblocking the valve or valve section, or by remaining in the blocked state and monitoring the data back signals from the valve electronics.

The test voltage U_{min} is defined as:

$$U_{min} = \frac{N_{tut}}{N_t} \times U_W \times k_2$$

where

U_W is the lowest DC voltage across one valve in service operation where proper function of the valve electronics is required;

N_{tut} is the number of series-connected VSC levels under test;

N_t is the total number of series-connected VSC levels in a single valve, including redundancy;

k_2 is a test safety factor;

k_2 = 0,95.

The duration of test shall be not less than 10 min.

7 Dielectric tests on valve support structure

7.1 Purpose of tests

The principal objectives of these tests are:

a) to verify the voltage withstand capability of the insulation of the valve support, cooling ducts, light guides and other insulating components associated with the valve support. If there is insulation to earth other than the valve support, then additional tests may be necessary;

b) to verify that the partial discharge inception and extinction voltages are above the maximum operating voltage appearing on the valve support.

NOTE Depending upon the application, it might be possible to eliminate some of the tests on the valve support, subject to agreement between purchaser and supplier.

7.2 Test object

The valve support to be used for the tests may be a representative separate object including representation of the adjacent parts of the valve or may form part of the assembly used for single valve or multiple valve unit tests. It shall be assembled with all ancillary components in place and shall have the adjacent earth potential surfaces properly represented. The proximity of adjacent earth potential surfaces (equipment or building infrastructure) shall be assessed, and representation included where appropriate. For clearances that are significantly greater than those determined by insulation co-ordination requirements, e.g. clearances driven instead by access requirements, then consideration may be given to omit earth potential surfaces in these locations. If a single valve consists of a single structure, then its large size may sometimes make it impractical to test the complete valve in a laboratory. In such cases it is permitted to perform the valve support structure tests on a pro-rated section of the support structure, provided it can be demonstrated that the design of the test object is representative of the design of the full structure and the tests cover the worst stresses experienced by any part of the valve support structure.

The coolant shall be in a condition representative of the most onerous service condition for the purpose of the test.

If a single valve consists of more than one structure such that there is more than one valve support structure per valve, then it shall be demonstrated that the tests proposed cover the worst stresses experienced by any of the valve support structures.

7.3 Test requirements

7.3.1 General

All test levels below are subject to atmospheric correction as described in 4.2.

7.3.2 Valve support DC voltage test

The two main terminals of the valve shall be connected together, and the DC voltage then applied between the two main terminals thus connected and earth. Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage as fast as possible, kept constant for 1 min, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero. During the last hour of the specified 3 h test, the number of partial discharges exceeding 300 pC shall be recorded as described in IEC 60700-1:2015 and IEC 60700-1:2015/AMD1:2021, Annex B.

The number of pulses exceeding 300 pC shall not exceed 15 pulses per minute, averaged over the recording period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity, the valve support may be short-circuited and earthed for a duration of several hours. The same procedure may be followed at the end of DC voltage test.

The valve support DC test voltage U_{tds} shall be determined in accordance with the following:

1 min test

$$U_{\text{tds}} = \pm U_{\text{dmS1}} \times k_3 \times k_{\text{t}}$$

3 h test

$$U_{\text{tds}} = \pm U_{\text{dmS2}} \times k_3$$

where

U_{dmS1} is the maximum short-duration voltage appearing across the valve support, as determined by insulation coordination studies. U_{dmS1} shall be the higher of (a) the highest voltage averaged over a 1 s period and (b) the average voltage during the time from the peak voltage to the time when the voltage decreases rapidly through the action of fast discharge devices or re-configuration, if any;

U_{dmS2} is the maximum value of the DC component of the steady-state operating voltage appearing across the valve support;

k_3 is a test safety factor;

k_3 = 1,10 for 1 min test;

k_3 = 1,15 for 3 h test;

k_{t} is the atmospheric correction factor according to 4.2.

7.3.3 Valve support AC voltage test

To perform the test, the two main terminals of the valve shall be connected together, and the AC test voltage then applied between the two main terminals thus connected and earth.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The valve support AC test voltage U_{tas} shall be determined in accordance with the following:

1 min test:

$$U_{tas} = \frac{U_{mS1}}{\sqrt{2}} \times k_4 \times k_t$$

30 min test

$$U_{tas} = \frac{U_{mS2}}{\sqrt{2}} \times k_4$$

where

U_{mS1} is the peak value of maximum voltage appearing on the valve support in service, particularly in system fault condition and valve fault operation condition. The overvoltage limiting effect of phase arrester or other overvoltage protection means, if any, shall be taken into account to derive this overvoltage;

U_{mS2} is the peak value of the maximum repetitive operating voltage across the valve support during steady-state operation, including switching overshoot;

k_4 is a test safety factor;

k_4 = 1,10 for 1 min test;

k_4 = 1,15 for 30 min test;

k_t is the atmospheric correction factor according to 4.2.

7.3.4 Valve support switching impulse test

The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltages between the main terminals of the valve (connected together) and earth.

A standard switching impulse voltage wave shape in accordance with IEC 60060 shall be used.

The test voltage shall be selected in accordance with the insulation coordination of the VSC substation.

7.3.5 Valve support lightning impulse test

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltages between the main terminals of the valve (connected together) and earth.

A standard lightning impulse voltage wave shape in accordance with IEC 60060 shall be used.

The test voltage shall be selected in accordance with the insulation coordination of the VSC substation.

8 Dielectric tests on multiple valve unit

8.1 General

This clause is only applicable if more than one valve is installed in a common valve structure (multiple valve unit). In the case where each individual valve is mounted in a dedicated valve structure, this clause is not applicable.

8.2 Purpose of tests

The principal objectives of these tests are:

a) to verify the voltage withstand capability of the external insulation of the MVU, with respect to its surroundings, especially for the valve(s) connected at pole potential;

b) to verify the voltage withstand capability between single valves in a MVU structure;

c) to verify that the partial discharge levels are within specified limits.

8.3 Test object

There are many possible arrangements of valves and multiple valve units. The test object(s) shall be chosen to reflect, as accurately as possible, the service configuration of valves insofar as is necessary for the test in question. The test object shall be fully equipped unless it can be shown that some components can be simulated or omitted without reducing the significance of the results.

Individual valves may have to be short-circuited depending on the configuration of the MVU and the objectives of the test.

When the low-voltage terminal of the MVU is not connected to earth potential, care shall be taken to suitably terminate the low voltage terminal of the MVU during tests to correctly simulate the voltage appearing at this terminal. Earth planes shall be used, whose separation shall be determined by the proximity of other valves and earth potential surfaces.

8.4 Test requirements

8.4.1 MVU DC voltage test to earth

The DC test voltage shall be applied between the highest potential DC terminal of the MVU and earth.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage as fast as possible, kept constant for 1 min, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

Where possible the test voltage shall be increased from 50 % to the 1 min test voltage level within approximately 10 s.

During the last hour of the specified 3 h test, the number of partial discharges exceeding 300 pC shall be recorded.

The number of pulses exceeding 300 pC shall not exceed 15 pulses per minute, averaged over the recording period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC, and no more than one pulse per minute shall exceed 2 000 pC.

If an increasing trend in the magnitude or rate of partial discharge is observed, the test duration may be extended by mutual agreement between the purchaser and supplier.

The test shall then be repeated with the voltage of opposite polarity.

Prior to the test and before repeating the test with voltage of opposite polarity, the MVU terminals may be short-circuited together and earthed for a duration of several hours. The same procedure may be followed at the end of DC voltage test.

The MVU DC test voltage U_{tdm} shall be determined in accordance with the following:

1 min test

$$U_{tdm} = \pm U_{dmm1} \times k_5 \times k_t$$

3 h test

$$U_{tdm} = \pm U_{dmm2} \times k_5$$

where

U_{dmm1} is the maximum short-duration voltage appearing between the high-voltage terminal of MVU and earth, as determined by insulation coordination studies. U_{dmm1} shall be the higher of (a) the highest voltage averaged over a 1 second period and (b) the average voltage during the time from the peak voltage to the time when the voltage decreases rapidly through the action of fast discharge devices or re-configuration, if any;

U_{dmm2} is the maximum value of the DC component of the steady-state operating voltage appearing between the high-voltage terminal of the MVU and earth;

k_5 is a test safety factor;

k_5 = 1,10 for 1 min test;

k_5 = 1,15 for 3 h test;

k_t is the atmospheric correction factor according to 4.2.

8.4.2 MVU AC voltage test

If a MVU experiences AC or composite AC plus DC voltage stresses between any two terminals, the withstand capability of which is not adequately demonstrated by other tests, then it will be necessary to perform an AC voltage test between these terminals of the MVU.

To perform the test, the test voltage source shall be connected to the pair of MVU terminals in question. The point of earth connection is dependent on the test circuit arrangement.

Starting from a voltage not higher than 50 % of the 1 min test voltage, the voltage shall be raised to the specified 1 min test voltage, kept constant for 1 min, then reduced to the 30 min value, kept constant for 30 min and then reduced to zero.

Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The MVU AC test voltage U_{tam} shall be determined in accordance with the following:

1 min test

$$U_{tam} = \frac{U_{mm1}}{\sqrt{2}} \times k_6 \times k_t$$

30 min test

$$U_{tam} = \frac{U_{mm2}}{\sqrt{2}} \times k_6$$

where

U_{mm1} is the peak value of maximum voltage between the terminals of the MVU in service, particularly in system fault condition and valve fault operation condition. The overvoltage limiting effect of phase arrester or other overvoltage protection means, if any, shall be taken into account to derive this overvoltage;

U_{mm2} is the peak value of the maximum repetitive operating voltage between the terminals of the MVU during steady-state operation, including switching overshoot;

k_6 is a test safety factor;

k_6 = 1,10 for 1 min test;

k_6 = 1,15 for 30 min test;

k_t is the atmospheric correction factor according to 4.2.

8.4.3 MVU switching impulse test

A standard switching impulse voltage waveshape in accordance with IEC 60060 shall be used.

The MVU switching impulse test voltage shall be applied between the high voltage terminal of the MVU and earth.

The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltage of a specified amplitude.

The MVU switching impulse test voltage U_{tsm} shall be determined in accordance with the following:

$$U_{tsm} = \pm U_{SIPL\_m} \times k_7 \times k_t$$

where

U_{SIPL_m} is the switching impulse protective level determined by insulation coordination taking into account the arrester(s) connected between the MVU high voltage terminal and earth;

k_7 is a test safety factor;

k_7 = 1,10;

k_t is the atmospheric correction factor;

k_t is the value according to 4.2.

If the test prescribed above does not adequately test the switching impulse withstand between all terminals of the MVU, then consideration shall be given to performing extra tests to check the insulation.

NOTE Subject to agreement between the purchaser and supplier, the MVU switching impulse test need not be performed if it can be shown by other means that:

a) the external air clearances to other valves and to earth are adequate for the switching impulse voltage withstand level required, and

b) the switching impulse withstand between any two terminals of the MVU is adequately demonstrated by other tests.

8.4.4 MVU lightning impulse test

A standard lightning impulse voltage wave shape in accordance with IEC 60060 shall be used.

The MVU lightning impulse test voltage shall be applied between the high voltage terminal of the MVU and earth.

The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltage of specified amplitude.

The MVU lightning impulse test voltage U_{tlm} shall be determined in accordance with the following:

$$U_{\text{tlm}} = \pm U_{\text{LIPL\_m}} \times k_8 \times k_t$$

where

$U_{\text{LIPL\_m}}$ is the lightning impulse protective level determined by insulation co-ordination, taking into account the arrester(s) connected between the MVU high voltage terminal and earth;

k_8 is a test safety factor;

k_8 = 1,10;

k_{t} is the atmospheric correction factor;

kt is the value according to 4.2.

If the test prescribed above does not adequately test the lightning impulse withstand voltage between all terminals of the MVU, then consideration shall be given to performing extra tests to check this insulation.

NOTE Subject to agreement between the purchaser and supplier, the MVU lightning impulse test need not be performed if it can be shown by other means that:

a) the external air clearances to other valves and to earth are adequate for the lightning impulse voltage withstand level required, and

b) the lightning impulse withstand voltage between any two terminals of the MVU is adequately demonstrated by other tests.

9 Dielectric tests between valve terminals

9.1 Purpose of the test

These tests are intended to verify the design of the valve regarding its voltage-related characteristics for various types of overvoltages (DC, AC, switching impulse and lightning impulse overvoltages). The tests shall demonstrate that:

a) the valve will withstand the specified overvoltages;

b) partial discharges will be within specified limits under specified test conditions;

c) the internal voltage grading circuits, if any, have sufficient power rating.

It should be noted that the tests described in this clause are based on standard wave shapes and standard test procedures as developed for the testing of high-voltage AC systems and components. This approach offers great advantages to the industry because it allows much of the existing technology of high-voltage testing to be carried over to the qualification of HVDC valves. On the other hand, it must be recognized that a particular HVDC application may result in wave shapes different from the standards and, in this case, the test may be modified so as to realistically reflect expected conditions.

It should be also noted that the atmospheric correction is not needed in dielectric tests between valve terminals if the site altitude is less than 1 000 m. However, for valves installed at an altitude exceeding 1 000 m the valve internal air clearance shall be verified by additional tests under the atmospheric corrected test voltages. IGBT-diode pairs can be replaced by insulating blocks in these tests.

9.2 Test object

For valves of the switch type, the test object should generally be a complete valve. For valves of the controllable voltage source type, testing a complete valve might not be practical because of its large physical size. In such cases the test object should generally be a single structure representative of valve dielectric design. Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections, under test conditions, is representative of the voltage distribution within a complete valve in service. The test valve or valve section shall be assembled with all auxiliary components except for the valve arrester if provided. The valve may form part of a multiple valve unit.

If a valve section is used as the test object, the minimum number of valve levels in the test section shall be agreed by the purchaser. In such cases, additional tests to verify the insulation between different parts of the complete valve may be needed and shall be agreed between purchaser and supplier.

The coolant shall be in a condition that represents service conditions except for flow rate which can be reduced. If any object external to the structure is necessary for proper representation of the stresses during tests, it shall be included or simulated in the test. The proximity of adjacent earth potential surfaces (equipment or building infrastructure) shall be assessed, and representation included where appropriate. For clearances that are significantly greater than those determined by insulation coordination requirements, e.g. clearances driven instead by access requirements, then consideration may be given to omit earth potential surfaces in these locations.

9.3 Test methods

9.3.1 General

VSC valves differ from line commutated converter (LCC) valves and other high-voltage equipment in several aspects. One of the most important differences is that the converter contains very large capacitive energy storage. For valves of the controllable voltage-source type, the storage is an integral part of the valve while for switch-type valves it is closely connected to the valve. The second major difference is the active voltage control at individual VSC valve levels. As a result of these characteristics, the test method used in LCC valve dielectric tests cannot be applied to such valves.

Performing the valve dielectric test presents considerable practical difficulties on controllable voltage source type VSC valves because of the high current drawn by those in-built capacitances. The very limited current ratings of available test supplies in practical high-voltage test laboratories mean that, without modifying the test object, an excessively long time is required to charge up the capacitance of the test object to the required voltage during the AC–DC voltage test, and this unreasonably over-stresses the test object. The very large capacitance

also makes measurement of partial discharges impossible, and impulse voltages between the valve terminals do not occur on a deblocked valve during operation. For this reason, two valve dielectric test methods, on the same principle, are defined for controllable voltage source type valve dielectric tests. Supplier can use either of them for the valve dielectric test.

Valve dielectric test on switch type VSC valves shall follow Method one.

9.3.2 Method one

Temporary substitution of a special test capacitor with reduced capacitance but the same housing as the original capacitor in each valve level is necessary if this method is used in test of controllable voltage source type valves. This test capacitor shall allow a test voltage build-up across the test object during test.

In addition, it may be necessary to disable gate electronics or other auxiliary circuits in this test or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

When gate electronics or other auxiliary circuits are disabled for the 10 s test, the active voltage control function, if any, provided by gate electronics or other auxiliary circuits on each IGBT level may be represented by other means, for example, high resistance shunt resistors across test IGBT levels for appropriate voltage sharing.

If it is not possible to disable gate electronics or other auxiliary circuits in this test and interference can be proven to be caused by electronics circuit, then this interference may be deducted from measurement.

9.3.3 Method two

Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections under test conditions, is representative of the voltage distribution within a complete valve in service.

In case of a controllable voltage source type VSC valve the active control of sub-module capacitor voltages equalises the voltage distribution across the complete valve. The in-built capacitances react as constant voltage sources with very low internal impedance. An impulse voltage will drive a high current, the resulting change of the sub-module voltage follows the tolerance of the in-built capacitor.

Valve dielectric test is done in single steps. Step one focuses on the component level and step two on the valve or valve section.

In step one, valve levels are tested independently. Insulation and partial discharge tests with AC, DC and/or combined AC–DC voltage shall be performed on sub-component level (e.g. without power module electronics activated and without capacitor) or on full submodule level. The aim is to demonstrate both the insulation withstand capability for every single sub-component and freedom from partial discharge for every sensitive point within the valve level.

As stated, the even distribution by actively controlled sub-module voltages allows to perform the dielectric test between valve terminals and also between tiers with adjusted test voltage levels.

Consequently, in step two, the test is done with submodule levels short-circuited, interconnections between adjacent submodules removed, and valve or valve section voltage distribution controlled by an external grading circuit, for example a resistor array, capacitor array or RC array.

The inter-tier structure represents a typical section of the tower structure. Essential components of the tower structure are exposed to the specified voltage values and shapes. Test of air clearance and creepage distances of tier insulators and capacitor's housing, fibre optics including their ducts, water cooling pipes and mechanical design. AC, DC (both including PD measurement) and impulse voltages will be tested. Additional safety margin to the specific test voltages is possible and used, e.g. atmospheric correction to the specific test voltages can be added.

NOTE The addition of external grading networks could modify the profile of the test object such that it is not fully representative of in-service equipment. Practically this could lead to difficulties in performing the test, especially in determining sources of partial discharge. Hence an alternative method can be used instead of fitting grading networks, where each insulation gap is tested independently at voltages relevant to each particular gap. This can be achieved by a combination of either removing interconnections and/or shorting out relevant parts of the test object, then applying the equivalent scaled voltage across the gap. The test is performed once for each design of insulation gap e.g. inter-tier, inter-stack, inter-sub-module. Where appropriate in the design, the test set-up also needs to consider diagonal gaps (gaps between sub-modules belonging to different stacks and different tiers, one above the other).

9.4 Test requirements

9.4.1 Composite AC-DC voltage test

This test reproduces the composite AC-DC voltage resulting from certain converter or system faults and in steady-state operation. The test consists of a short-duration test and a long-duration test.

In this test, a capacitor can be used in conjunction with an AC test voltage source to produce a composite AC-DC voltage waveform. Depending on the converter topology, the capacitor could be an integral part of the valve, or it could be a separate item (part of the test circuit, not part of the test object).

Alternatively, a separate DC voltage source could be used to substitute the capacitor.

Starting from a voltage not higher than 50 % of the 10 s test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For AC PD (partial discharge) measurement, the level of partial discharge recorded during the last minute of the 3 h test shall be less than 200 pC, provided that the components which are sensitive to partial discharge in the valve have been separately tested. For DC PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

NOTE 1 If an increasing trend in the rate or magnitude of partial discharge is observed, the test duration might be extended by mutual agreement between the purchaser and supplier.

NOTE 2 It may be necessary to disable gate electronics or other auxiliary circuits in this test, or provide independent means for powering them, in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

The valve test voltages have a sinusoidal waveshape superimposed on a DC level.

The valve 10 s test voltage U_{tv1} shall be determined in accordance with the following:

$$U_{tv1} = (k_{c1} \times U_{tac1} \times \sin(2\pi ft) + U_{tdc1}) \times k_0 \times k_9$$

where

U_{tac1} is the peak value of the AC component of maximum temporary overvoltage appearing between the terminals of the valve, calculated from the peak-to-peak valve voltage divided by two;

U_{tdc1} is the maximum of 1 s average value of the DC component of voltage appearing between the terminals of the valve at faults, after taking into account of voltage limiting effect of DC pole surge arrester;

k_{c1} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac1}. For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

k_0 is a test scaling factor according to 4.3.2;

k_9 is a test safety factor;

k_9 = 1,1;

f is the test frequency (50 Hz or 60 Hz depending on test facilities).

NOTE 3 The conditions leading to the highest values of U_{tac1} and U_{tdc1} might not occur simultaneously. When performing a combined AC–DC test it is important to use self-consistent conditions that lead to the worst combined valve stress, in order to avoid over-stressing, the test object. For the 10 s test, the most important parameter is generally the peak of the combined voltage.

The valve 3 h test voltage U_{tv2} shall be determined in accordance with the following:

$$U_{tv2} = U_{tac2} + U_{tdc2}$$

$$U_{tac2} = U_{max-cont} \times \sin(2\pi ft) \times k_{c2} \times k_0 \times k_9$$

$$U_{tdc2} = U_{dmax} \times k_0 \times k_9$$

where

$U_{max\text{-}cont}$ is the peak value of the AC component of steady-state voltage appearing between the terminals of the valve, calculated from the peak-to-peak valve voltage divided by two;

U_{dmax} is the maximum value of the DC component of the steady-state operating voltage between the terminals of the valve, calculated from the voltage between the DC terminals of the converter divided by two;

k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2}. For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

f is the test frequency (50 Hz or 60 Hz depending on test facilities).

9.4.2 Alternative tests (Method 2 only)

9.4.2.1 General

When method two is adopted, the composite AC-DC voltage test specified in the previous sub-clause may be replaced, during step two, by an AC voltage test and an DC voltage test performed separately.

NOTE It is generally only possible to apply the alternative test method when testing passive insulation gaps, since the freewheel diodes in the valve will normally prevent the application of a pure AC voltage.

9.4.2.2 Valve AC voltage test

The test consists of applying the specified test voltages U_{tac1} and Ut_{ac2} for the specified duration. U_{tac1} and U_{tac2} have sinusoidal waveshapes with a frequency of 50 Hz or 60 Hz, depending on the test facility.

The test will be done with a short duration of 10 s and a long duration of 30 min.

Starting from a voltage not higher than 50 % of the 10 s test voltage, the voltage shall be raised to the specified 10 s test level, kept constant for 10 s, reduced to the specified 30 min test voltage, kept constant for 30 min and then reduced to zero. Before the end of the 30 min test, the level of partial discharge shall be monitored and recorded over a 1 min period. If the value of partial discharge is below 200 pC, the design may be accepted unconditionally. If the value of partial discharge exceeds 200 pC, the test results shall be evaluated.

The RMS value of valve 10 s AC test voltage, U_{tac1}, and 30 min AC test voltage, U_{tac2}, shall be determined in accordance with the following:

$$U_{tac1} = \frac{U_{vp1}}{\sqrt{2}} \times k_{c1} \times k_0 \times k_{10}$$

$$U_{tac2} = \frac{U_{vp2}}{\sqrt{2}} \times k_{c1} \times k_0 \times k_{10}$$

where

U_{vp1} is the peak value of the maximum temporary overvoltage across the valve;

U_{vp2} is the peak value of the maximum steady-state voltage across the valve;

k_{c1} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac1}. For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

k_{c2} is the voltage step overshoot factor related to one output voltage step of the converter, under the condition consistent with that used to define U_{tac2}; For a MMC or CTL type converter the voltage step overshoot factor relates to the overshoot factor of one cell or submodule;

k_0 is the test scaling factor according to 4.3.2;

k_{10} is a test safety factor;

k_{10} = 1,10.

9.4.2.3 Valve DC voltage test

The test consists of applying the specified test voltages U_{tdc1} and U_{tdc2} for the specified duration.

The test will be done with a short duration of 10 s and a long duration of 3 h.

Starting from a voltage not higher than 50 % of 10 s test voltage, the voltage shall be raised to the specified 10 s test level as fast as possible, reduced to the specified 3 h test voltage, kept constant for 3 h and then reduced to zero.

For DC PD measurement the recording time shall be the last hour of the 3 h test. The number of pulses exceeding 300 pC shall not exceed 15 per minute, averaged over the record period. Of these, no more than seven pulses per minute shall exceed 500 pC, no more than three pulses per minute shall exceed 1 000 pC and no more than one pulse per minute shall exceed 2 000 pC.

The valve 10 s DC test voltage, U_{tdc1}, and 3 h DC test voltage, U_{tdc2}, shall be determined in accordance with the following:

$$U_{tdc1} = U_{vp1} \times k_0 \times k_{10}$$

$$U_{tdc2} = U_{vp2} \times k_0 \times k_{10}$$

9.4.3 Valve impulse tests

9.4.3.1 General

The following shall be taken into account during valve impulse tests.

a) For some applications, for instance no overhead line is present in DC side and the busbar between phase reactor and valves is completely protected against direct lightning strike in AC side or in topologies, where the valve acts as a controllable voltage source with its own inbuilt DC capacitance, the valve impulse tests are less important since the valves do not see impulses at an amplitude which could be decisive in the electric performance of valves. Impulse tests in such applications can be omitted.

   NOTE 1 Unless all equipment between the transformer and DC reactors are completely enclosed, the possibility of lightning striking an exposed section of busbar adjacent to the valve (for example between the valve reactors and the valve) cannot be excluded. However, taking into account the small area affected and the low probability of having a lightning impulse of magnitude low enough to evade the shielding, this event is extremely unlikely to occur in practice and can therefore be ignored.

   NOTE 2 The emergency turn-off of the IGBT valve while it is carrying current (IGBT overcurrent turn-off test: Clause 10) can also generate a transient overvoltage between the terminals of the valve. Part of this overvoltage appears directly across the valve levels and is covered by the IGBT overcurrent turn-off test but there might, in addition, be a transient voltage developed across the stray inductance of the busbars through the valve which might need to be considered in the assessment of impulse voltage stresses between terminals.

b) The impulse test will be applied only in one polarity which corresponds to the polarity of valve withstand voltage.

c) If the valve impulse withstand levels are equal to or less than the valve AC-DC test level, it is deemed that the valve AC-DC test can cover the impulse tests and consequently the impulse tests can be omitted.

9.4.3.2 Valve switching impulse test

A standard switching impulse voltage waveshape in accordance with IEC 60060 shall be used.

The test shall comprise three applications of switching impulse voltages of specified amplitude on the valve.

The valve switching impulse test withstand voltage U_{tsv} shall be determined in accordance with the following:

– Valve with valve arrester protection:

$$U_{tsv} = U_{SIPL\_v} \times k_0 \times k_{11}$$

where

U_{SIPL_v} is the switching impulse protective level of valve arrester or protection level derived from AC and DC side arresters;

k_0 is a test scaling factor according to 4.3.2;

k_{11} is a test safety factor;

k_{11} = 1,10.

– Valve without valve arrester protection:

This test is intended to verify the valve insulation when the valve is not directly protected by surge arresters.

$$U_{tsv} = U_{cms} \times k_0 \times k_{12}$$

where

U_{cms} is the switching impulse prospective voltage across valve terminals according to system insulation coordination studies;

k_0 is a test scaling factor according to 4.3.2;

k_{12} is a test safety factor;

k_{12} = 1,15.

The valve shall withstand the test voltage without switching or insulation breakdown.

9.4.3.3 Valve lightning impulse test

A standard lightning impulse voltage waveshape in accordance with IEC 60060 shall be used.

The test shall comprise three applications of impulse voltages of specified amplitude on the valve.

The valve lightning impulse withstand voltage U_{tlv} shall be determined in accordance with the following.

– Valve with valve surge arrester protection:

$$U_{tlv} = U_{LIPL\_v} \times k_0 \times k_{13}$$

where

U_{LIPL_v} is the lightning impulse protective level of the valve arrester or protection level derived from AC and DC side arresters;

k_0 is a test scaling factor according to 4.3.2;

k_{13} is a test safety factor;

k_{13} = 1,10.

– Valve without valve surge arrester protection:

This test is intended to verify the valve insulation when the valve is not directly protected by surge arresters.

$$U_{\text{tlv}} = U_{\text{cml}} \times k_0 \times k_{14}$$

where

U_{cml} is the lightning impulse prospective voltage across valve terminals according to system insulation coordination studies;

k_0 is a test scaling factor according to 4.3.2;

k_{14} is a test safety factor;

k_{14} = 1,15.

The valve shall withstand the test voltage without switching or insulation breakdown.

10 IGBT overcurrent turn-off test

10.1 Purpose of test

The principal objective is to check the adequacy of the VSC valve design, especially the IGBT, and the associated electrical circuits with regard to current and voltage stresses at turn-off in the event of certain short circuit faults or misfiring events.

The test shall replicate the worst combination of voltage stress and instantaneous junction temperature, based on conditions that represent the most unfavourable tolerance settings of the monitoring/protection circuits. Depending on the control and protection strategy more than one test may be required in order to reproduce all relevant stresses.

General requirements related to the test circuit and the representation of DC capacitor, loop stray inductance, etc. are as stated in 6.3.

10.2 Test object

The test object is as described in 6.2. However, it is also necessary to represent certain protection or monitoring circuits if these are essential for the detection of an overcurrent event. For controllable voltage source type VSC valves, this test may also be performed on valve level.

10.3 Test requirements

The test consists of operating the test object to thermal equilibrium under the conditions which lead to the highest steady-state junction temperature of the relevant IGBT (see 6.4) and then initiating an overcurrent event. The control and protection system then detects the overcurrent and suppresses the overcurrent by turning off the IGBTs at a current below the maximum safe turn-off limit.

For switch type valve, the test voltage U_{tpv2} shall be determined as follows:

$$U_{tpv2} = U_{dtemp} \times k_n \times k_{15}$$

where

U_{dtemp} is the maximum temporary DC overvoltage of the valve, including ripple;

k_n is a test scaling factor according to 4.3.1;

k_{15} is a test safety factor;

k_{15} = 1,05.

For controllable voltage source type valve, the test voltage U_{tpvl2} per valve level shall be determined as follows:

$$U_{tpvl2} = U_{ctemp} \times k_{15}$$

where

U_{ctemp} is the maximum temporary DC overvoltage per valve level, including ripple;

k_{15} is a test safety factor;

k_{15} = 1,05.

The rate-of-rise di/dt of the overcurrent shall be taken into consideration in the test to show that the control and protection system is able to turn-off the IGBTs fast enough before maximum safe turn-off limits are reached. This consideration can be shown either by increasing the rate-of-rise di/dt of the test current waveform if the test circuit allows for it or by increasing the protection level by taking into consideration of the total inherent delay in the control and protection system.

11 Short-circuit current test

11.1 Purpose of tests

The principal objective is to check the adequacy of the devices, especially the diodes, any additional components used to protect the diodes (such as bypass thyristors) and the associated electrical circuits with regard to current stresses under specified short circuit conditions, such as short-circuit fault at DC side, until the control and protection circuit breaks the fault current. The VSC valves shall be designed to withstand the short circuit overcurrent for the number of cycles needed to open the main AC circuit breaker, without any failure or damage in the equipment, considering also that a possible recovery voltage could appear. Valve electronics shall normally be energized for the part of the fault event where any actions are taken by it. For example, when blocking the IGBTs or turning on protective devices such as bypass thyristors. For other parts of the fault event, it is not necessary to energize the valve electronics.

11.2 Test object

The test object is as described in 6.2.

11.3 Test requirements

The test consists of operating the test object to thermal equilibrium under the conditions which lead to the highest steady-state junction temperature of the relevant semiconductor component (see 6.4) and then initiating a fault current event. In order to define the maximum junction

temperature rise of the IGBTs and the diodes, all the possible overload conditions (in terms of amplitude and duration) shall be taken into consideration.

The fault current amplitude, duration and the number of cycles shall be the maximum values expected in the actual field operation.

Alternative test waveform may be used, provided that the amplitude and energy accumulation are representative of those in fault conditions.

Where the test object experiences a recovery voltage between cycles of fault current, then this recovery voltage, including commutation overshoot where applicable, shall also be reproduced during the test. A test safety factor of 1,05 is applied to the recovery voltage.

Considering the difficulty in test laboratory to perform this test in generation of the recovery voltage between cycles of fault current, this test may, subjected to the agreement between purchaser and supplier, be performed on component level.

12 Tests for valve insensitivity to electromagnetic disturbance

12.1 Purpose of tests

The principal objective is to demonstrate the insensitivity of the valve to electromagnetic interference (electromagnetic disturbance) arising from voltage and current transients generated within the valve and imposed on it from the outside. The sensitive elements of the valve are generally electronic circuits used for controlling, protection and monitoring of the valve levels.

Generally, the valve insensitivity to electromagnetic disturbance can be checked by monitoring the valve during other type tests. Of these, the valve maximum continuous operating duty test and maximum temporary overload operating duty test (see 6.4 and 6.5), the valve impulse tests (see 9.4.3) and the IGBT overcurrent turn-off test (see Clause 10) are the most important.

The tests shall demonstrate that:

a) out-of-sequence or spurious switching of IGBT does not occur;

b) the electronic protection circuits installed in the valve operate as intended;

c) false indication of valve level faults or erroneous signals sent to the converter control and protection systems by the valve base electronics, arising from receipt of false data from the valve monitoring circuits, does not occur.

NOTE For this document, tests to demonstrate valve insensitivity to electromagnetic disturbance apply only to the VSC valve and that part of the signal transmission system that connects the valve to earth. Demonstration of the insensitivity to electromagnetic disturbance of equipment located at earth potential and characterization of the valve as a source of electromagnetic disturbance for other equipment are not within the scope of this document.

12.2 Test object

Generally, the test object is the valve or valve sections as used for other tests.

When insensitivity to electromagnetic disturbance arising from coupling between adjacent valves in a MVU is to be demonstrated, two approaches are acceptable as defined in 12.3. In this case, the test object will be a separate valve or valve section according to the approach adopted.

12.3 Test requirements

12.3.1 General

When demonstrating insensitivity to electromagnetic disturbance arising from coupling between adjacent valves of a MVU, the test requirements depend on which of the two recommended approaches is adopted.

The specific geometric arrangement to be used and the magnitude of the forward voltage for the electromagnetic disturbance test object shall be representative of the service conditions.

12.3.2 Approach one

Approach one is to simulate the source of electromagnetic disturbance directly as part of a test set-up. Such a test set-up will require more than one valve or valve section in order to check for interaction between them. The geometric arrangements of the source of the electromagnetic disturbance with respect to the valve under test shall be as close as possible to the service arrangement (or worse from an electromagnetic disturbance point of view). The electronics of the electromagnetic disturbance test object shall be energized. Those parts of the valve base electronics that are necessary for the proper exchange of information with the electromagnetic disturbance test object shall be included.

12.3.3 Approach two

Approach two is to determine the intensity of electromagnetic fields under worst operational conditions, either from theoretical considerations or by measurements. In a second step, these fields are simulated by a test circuit which generates correct (or worse) electromagnetic radiation at the respective frequencies. A valve section is then exposed to the fields generated by the test source.

An essential prerequisite to approach two is the determination of the dynamic field strength and direction at key locations in the valve. This can generally be obtained from search coil measurements taken during firing tests on a single valve. Alternatively, the field can be predicted from three-dimensional field modelling programs. A valve section shall then be tested using a separate field coil to produce field intensity, frequency content and direction which is at least as severe as the predicted values.

The following conditions for the valve section under test shall be met:

– the valve section shall have operational voltage (proportionally scaled) between its terminals and be forward biased at the time of energization of the field coil;
– the electronics of the valve section under test shall be energized;
– those parts of the valve base electronics that are necessary for the proper exchange of information with the valve section shall be included.

12.3.4 Acceptance criteria

The criteria for acceptance for both approaches one and two shall be as defined in 12.1.

13 Tests for dynamic braking valves

In some VSC HVDC schemes, but particularly where the HVDC system is exporting power from a small islanded AC system with little or no load (for example an offshore wind farm) the HVDC system may be required to include a dynamic braking system, for example as a chopper connected to the DC terminals of the VSC system. The function of the dynamic braking system is to absorb and dissipate the power generated in the islanded AC system during faults in the receiving-end AC system, typically for durations of 1 s to 2 s.

There are several possible ways of implementing such a dynamic braking system but the valves in this system will, in general, be of similar design to the main VSC valves used for power transmission.

The dynamic braking valves may require type tests, for which the requirements given in the preceding Clauses 6 to 12 are generally applicable; however, the dynamic braking valves generally require only a sub-set of the type tests applicable to VSC valves.

The dynamic braking valve normally remains in the standby state but is required to operate and carry current for short durations when the receiving-end AC system suffers a fault. The dielectric test conditions are therefore similar to those for the VSC valve but the operational test conditions only need to be applied for short durations.

NOTE 1 Subclause 4.1.1, *Evidence in lieu*, is applicable when the same valve design is used in both VSC valve and dynamic braking valve.

NOTE 2 For dynamic braking valve with a design of distributed in-built resistors or energy absorber element the operational duties can be done on site, due to the power limitation of test laboratory.

14 Production tests

14.1 General

This clause covers tests on assemblies of components that are parts of valves, valve sections, or auxiliary circuits for their protection, control and monitoring. It does not cover tests on individual components that are used within the valve, the valve support, or valve structure.

For valve component fault tolerance, information is provided in Annex B.

14.2 Purpose of tests

The purpose of the production tests is to verify proper manufacture by demonstrating that:

– all components and subassemblies used in the valve have been correctly installed in accordance with the design;
– the valve equipment functions as intended and predefined parameters are within prescribed acceptance limits;
– the valve sections and IGBT-diode pair levels (as appropriate) have adequate voltage withstand capability;
– consistency and uniformity in production is achieved.

14.3 Test object

All valve sections or parts thereof manufactured for the project shall be subjected to the routine production tests. The tests may be performed on valve sections or individual levels as appropriate to the design and available test facilities.

14.4 Test requirements

Uniformity in the specified production tests of different suppliers is unnecessary. The production tests shall take into account the special design characteristics of the valve and its components, the extent to which the components are tested prior to assembly, and the particular manufacturing procedures and techniques are involved. In this clause, only production test objectives are given.

In all cases, the supplier shall submit, for approval by the purchaser, a detailed description of the test procedures proposed to meet the production test objectives.

The minimum requirements for routine production tests are listed in 14.5. The order in which the tests are listed implies neither ranking of importance nor the order in which the tests shall be performed.

In some cases, it may be necessary to perform production sample tests on complete assemblies in addition to the routine tests, for example when modifications are introduced in the course of production. The nature and extent of such additional tests shall be agreed on a case-by-case basis.

14.5 Production test objectives

14.5.1 Visual inspection

To check that all materials and components are undamaged and are correctly installed in accordance with the latest approved revision of the production documentation.

14.5.2 Connection check

To check that all the main current-carrying connections have been made correctly.

14.5.3 Voltage-grading circuit check

To check the grading circuit parameters and thereby ensure that voltage division between series-connected levels will be correct for applied voltages from DC to impulse waveshapes, if applicable.

14.5.4 Control, protection and monitoring circuit checks

To check the function of any control, protection or monitoring circuits that form an integral part of the valve, such as IGBT gate drive circuits and any local protection or monitoring circuits.

If type tests and tests of the effectiveness of fuse protection are considered to be necessary, they shall be specified separately with conditions for tests.

14.5.5 Voltage withstand check

To check that the valve components can withstand the voltage corresponding to the maximum value specified for the valve. The checks shall include AC–DC test voltage and switching impulse as applicable.

14.5.6 Turn-on / turn-off check

To check that the IGBT(s) in each valve level turns on and turn off correctly in response to switching commands.

14.5.7 Pressure test

To check that there are no coolant leaks.

15 Presentation of type test results

The type test report shall be issued in accordance with the general guidelines as given in ISO/IEC 17025, and shall include the following information:

– name and address of the laboratory and location where the tests were carried out;
– name and address of the purchaser;
– unambiguous identification of the test object, including type and ratings, serial number and any other information aimed to identify the test object;
– dates of performance of the tests;
– description of test circuits and test procedures used for the performance of the tests;
– reference to the normative documents and clear description of deviations, if any, from procedures stated in the normative documents;
– description of measuring equipment and statement of the measuring uncertainty;
– test results in the form of tables, graphs, oscillograms, and photographs as appropriate;
– description of equipment or component failure;
– other data/statement/description as intention of evidence in lieu.

Annex A
(informative)

Overview of VSC converters in HVDC power transmission

A.1 General

Voltage sourced converter (VSC) valves are an evolving technology, in which different manufacturers may have substantially different technological approaches and where, in the future, there may be new circuit topologies that have not yet been described.

Voltage sourced converters for HVDC differ fundamentally from conventional HVDC converters (which are line commutated converters) in that in order to reverse the direction of power flow, it is the direction of direct current, not the polarity of direct voltage, that is reversed. Smoothing of the direct voltage is performed by a large DC capacitor, which plays an analogous role to the DC inductor (which may partly be fulfilled by the inductance of the DC transmission system and the leakage inductance of the converter transformers) in a conventional HVDC project.

In fact, in a great many respects, the role of voltage in a VSC valve is equivalent to that of current in a conventional HVDC thyristor valve, and vice-versa.

A detailed treatment of all possible VSC valve technologies is far beyond the scope of this standard. The purpose of this annex is simply to present a brief overview of the main differences between VSC and conventional HVDC thyristor valves, and of the main types of VSC valve, insofar as they affect the criteria for testing such valves.

This annex is intended to give an overview of the main converter technologies known at the time of writing. However, it is not intended to limit or constrain in any way the types of technology that can be utilized.

For determination and evaluation of the VSC valve losses, information is provided in Annex C.

A.2 VSC basics

All voltage sourced converters aim to synthesize, from the DC capacitor voltage, an approximately sinusoidal voltage at the AC terminals. However, in practice, the output voltage of the VSC cannot be perfectly sinusoidal but instead consists of a number of discrete steps of voltage, or "output levels". The term "level" here refers to a discrete output voltage level and should not be confused with the term "VSC valve level" which refers to a physical building-block of the valve, for example an individual IGBT and associated components.

For power systems, 3-phase converters are almost always used, but in considering the number of output levels of a converter, each "phase unit" of the converter is normally considered independently. The number of output levels refers to the number of discrete states in which the line-to-neutral output voltage of a phase unit can exist (Figure A.1). It is important to note that an *n*-level converter will have ($2n$-1) possible values of line-to-line voltage.

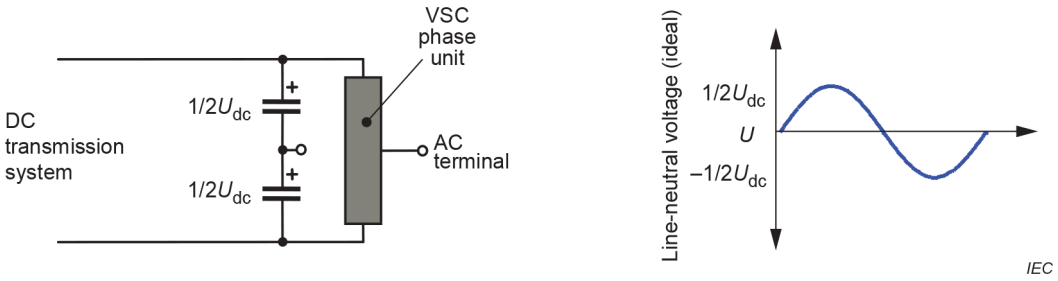
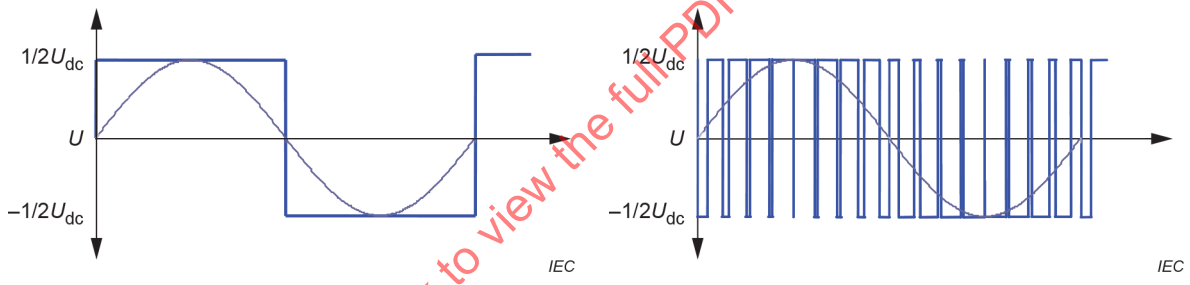


Figure A.1 – A single VSC phase unit and its idealized output voltage

In the simplest possible VSC topology, the "two-level converter", the AC output voltage of each phase arm (with respect to the midpoint of the DC capacitor, which is normally earthed) has only two possible states: $+½U_{dc}$ and $–½U_{dc}$.

If the VSC valves in this phase arm are switched only at fundamental frequency, the resulting AC output voltage waveform is an extremely poor approximation to sinusoidal. Such a waveform would be totally unacceptable in a power system.

However, by switching the valves ON and OFF more than once per fundamental frequency cycle and employing pulse width modulation (PWM) it is possible to obtain an output voltage that is, after filtering, reasonably sinusoidal. Figure A.2 illustrates both cases.



a) Without PWM b) With PWM

Figure A.2 – Output voltage of a VSC phase unit for a 2-level converter

PWM is an established technique in converters for motor drives, but carries the disadvantage of much increased switching losses.

An alternative to PWM is to use a more complex converter with a higher number of output levels – a "multi-level converter". There are a number of 3-level or 5-level converter topologies available, but in a power system application these too will generally still require PWM in order to obtain sufficiently low harmonics.

However, there are some converter topologies that are capable of producing much higher numbers of output levels, such that even without using PWM, the output voltage waveform is highly sinusoidal and little or no filtering is required. Figure A.3 shows the output voltage of a 15-level converter, which can be seen to be reasonably sinusoidal. In practice, higher numbers of levels than 15 would normally be used for HVDC transmission applications.

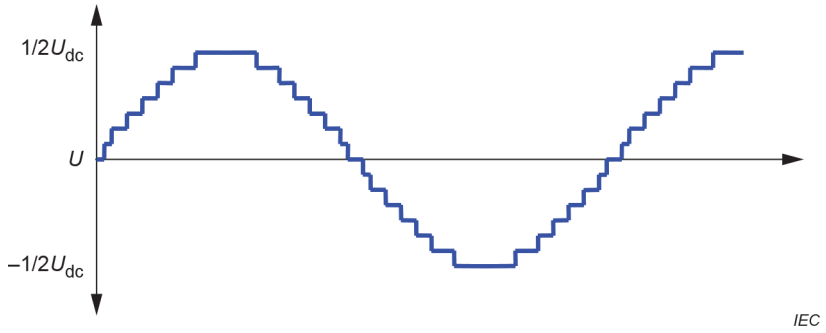


Figure A.3 – Output voltage of a VSC phase unit for a 15-level converter, without PWM

A.3 Overview of main types of VSC valve

Unlike conventional HVDC thyristor valves, which have evolved towards a largely common overall design, VSC valves are at an early stage in their technological evolution and exist in a number of forms.

At the time of writing of this standard, the VSC valves that are available commercially fall into two basic categories.

- Switch type VSC valves. These valves, like their thyristor counterparts, function only as a controllable switch, with only two permanent states: ON and OFF. In converters based on this topology, the DC capacitors are completely separated from the valves and can be tested in isolation.
- Controllable voltage source type VSC valves. In valves of this type, the DC capacitors form an integral part of the valve and cannot conveniently be separated from it for testing purposes.

Certain type tests need to be performed in a quite different way depending on which of the above categories the valve falls into.

Some other categories of "hybrid" VSC valve have also been described in literature and exhibit a mixture of characteristics from the two categories above; however at the time of writing, development work in these topologies is in the relatively early stages and these topologies are not yet commercially available.

A.4 Switch type VSC valve

A.4.1 General

VSC valves of this type bear a close apparent resemblance to conventional thyristor valves, in that they consist of a large number of series connected IGBT devices which are switched simultaneously. As with conventional thyristor valves, simultaneous switching of the series connected IGBTs is vital. Redundancy can be provided in the same way as for an LCC thyristor valve, by providing a few additional IGBT devices in series and either ensuring that the IGBTs are of a special type with short-circuit failure mode or are equipped with a parallel-connected shorting switch.

Valves of this type are normally used with converters with a relatively low number of output levels. To compensate for the low number of output levels, such converters usually use pulse width modulation (PWM) to achieve a good approximation of a sinusoidal output voltage.

Some of the more common converter topologies that can be used with this type of VSC valve are described below.

A.4.2 2-level converter

In this, the simplest type of VSC, each VSC phase unit comprises just two VSC valves connected in series and sharing an AC terminal. The two valves are switched alternately such that, at any given time, either one or the other valve is conducting, but never both. (In practice, there is usually a slight dead-time or "underlap" between the two valves in order to prevent a "shoot-through" or simultaneous conduction of the two valves in series).

The circuit topology of this converter is very simple (see Figure A.4) and requires very little explanation. When V1 is conducting, the AC terminal is connected to the upper DC terminal and therefore produces an output voltage of $+½U_{dc}$. When V2 is conducting, the AC terminal is connected to the lower DC terminal and therefore produces an output voltage of $–½U_{dc}$.

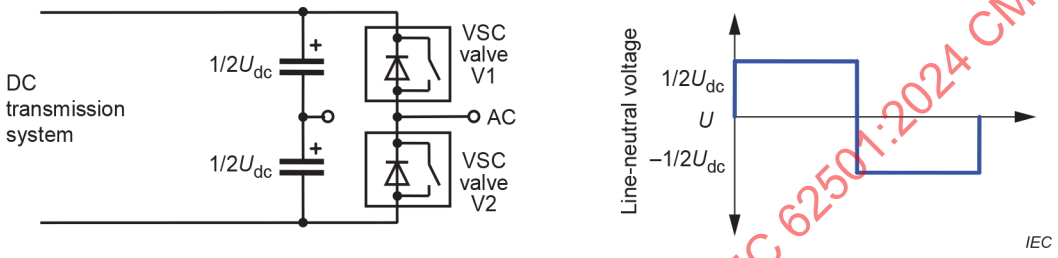


Figure A.4 – Basic circuit topology of one phase unit of a 2-level converter

A.4.3 Multi-level diode clamped converter

In this family of converters, the DC capacitor is sub-divided into a number of discrete stages connected in series, more than two IGBT valves are provided per phase unit and diode valves are used to connect between various intermediate points in the DC capacitor and in the phase unit.

In the simplest version of this circuit (see Figure A.5), the three-level converter, each phase unit contains four independent VSC valves connected in series. The DC capacitor is subdivided into two series-connected units (as it frequently is for a 2-level converter). The AC terminal is connected to the terminal between V2 and V3, and the ¼ and ¾ points (between valves V1/V2 and V3/V4) are connected to the DC midpoint via diode valves.

With this converter, three output states are possible from a single phase unit. When valves V1+V2 are conducting, the AC terminal is connected to the upper DC terminal and therefore produces an output voltage of $+½U_{dc}$. When valves V3+V4 are conducting, the AC terminal is connected to the lower DC terminal and therefore produces an output voltage of $–½U_{dc}$. When valves V2+V3 are conducting, the AC output voltage is "clamped" at the DC midpoint voltage by the diode valves.

The same principle can be extended to higher numbers of levels by further subdividing the DC capacitor and using more VSC and diode valves. In a 5-level converter, the DC capacitor is subdivided into four discrete stages, and there are eight VSC valves and six diode valves (see Figure A.6). In this circuit, the valves are switched in adjacent groups of four, for example V1+V2+V3+V4 gives an output voltage of $+½U_{dc}$, V2+V3+V4+V5 gives an output voltage of $+¼U_{dc}$, etc.

It can be seen that as the number of output levels increases, the complexity of the circuit increases disproportionately. This is made worse by the fact that not only the number, but also the voltage rating of the diode valves increases rapidly with the number of output levels.

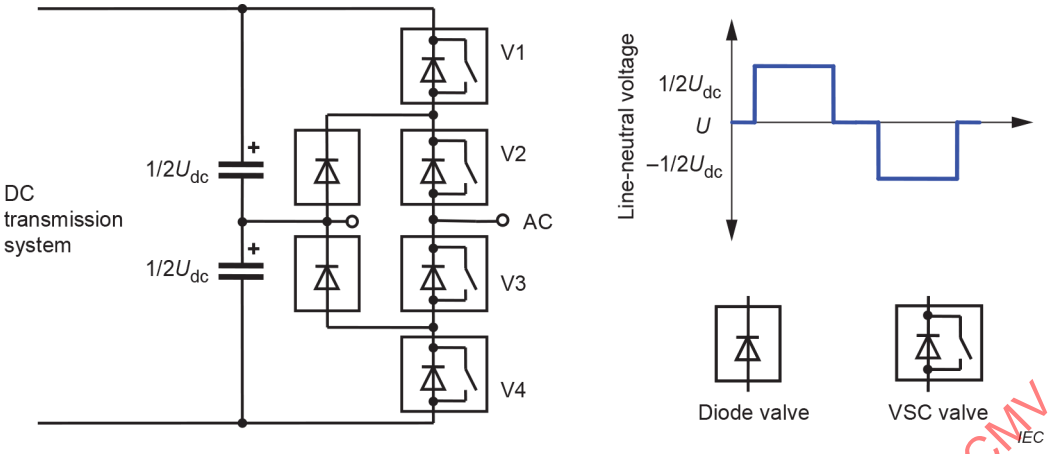


Figure A.5 – Basic circuit topology of one phase unit of a 3-level diode-clamped converter

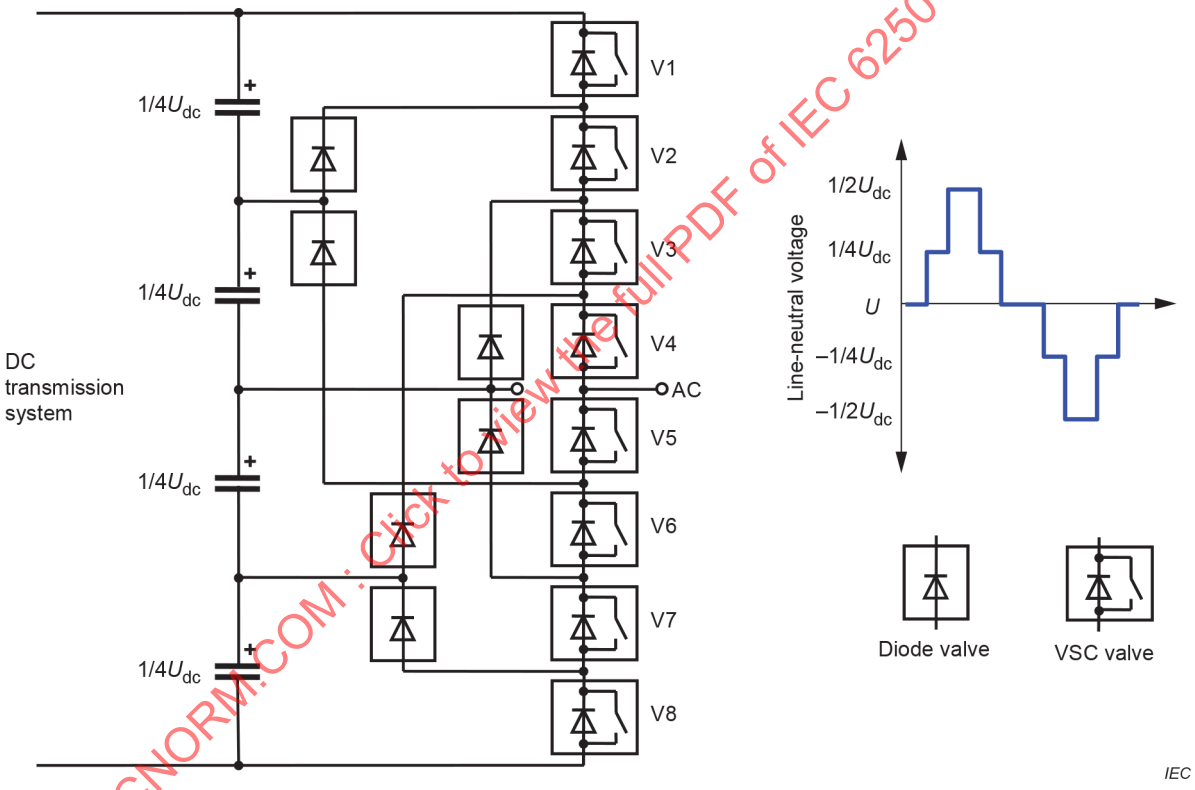


Figure A.6 – Basic circuit topology of one phase unit of a 5-level diode-clamped converter

A.4.4 Multi-level flying capacitor converter

This circuit achieves the same result as the diode-clamped converter by a different method. Instead of using diode valves to clamp the output voltage to one of the intermediate DC capacitor stages, it uses one or more additional DC capacitors, which are isolated from the DC terminals and hence "floating" or "flying", to achieve the same effect. This circuit is sometimes also referred to as the "Foch-Meynard" circuit after its inventors.

The 3-level flying capacitor converter (see Figure A.7) has a single flying capacitor with a nominal voltage of ½U_{dc}. This capacitor is connected between the terminals shared by V1/V2 and those shared by V3/V4. As with the 3-level diode-clamped converter, valves are switched in pairs but the pattern to achieve zero output voltage is different. To achieve an output state of 0, either valves V1+V3 or valves V2+V4 are switched on. V2+V3 is an illegal combination as it would short-circuit the flying capacitor.

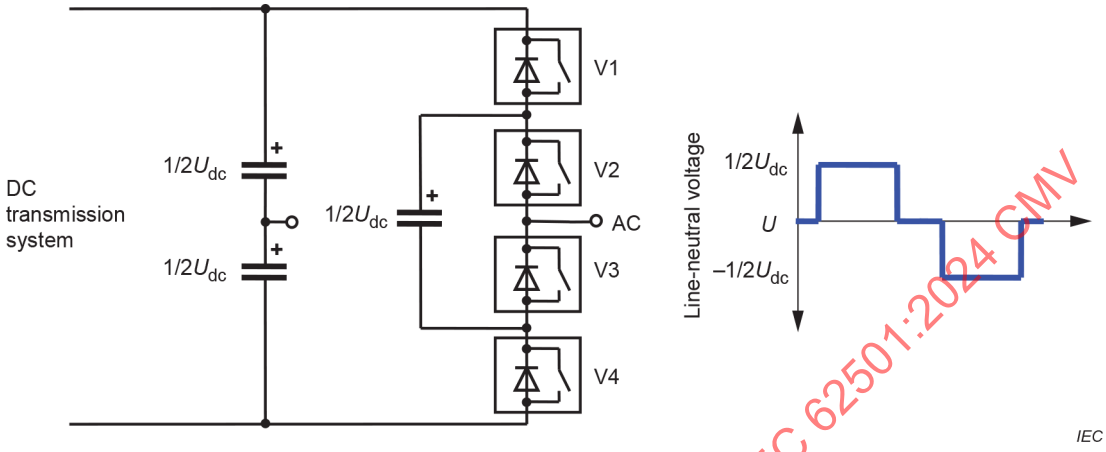


Figure A.7 – Basic circuit topology of one phase unit of a 3-level flying capacitor converter

The number of VSC valves per phase unit is the same for this converter as it is for a diode-clamped converter with the same number of output levels. Like the diode-clamped converter, higher numbers of output levels are possible, but at the expense of disproportionately increased complexity.

A.5 Controllable voltage source type VSC valve

A.5.1 General

In the 2-level converter, the valves and DC capacitor are clearly separated items of equipment and can be designed and tested in isolation. However, as the number of output levels increases, it is seen from Subclauses A.4.3 and A.4.4 that the DC capacitor(s) become increasing subdivided and the valves and DC capacitor become increasingly inter-dependent.

As the converter starts to approach the ideal, where the number of output levels is sufficient to obtain a good approximation to a sinusoidal waveform without using PWM, the subdivision of the DC capacitor and the interconnectivity between capacitors and IGBTs can become so complex that it is no longer practical to make a clear distinction between the two. In such cases, it may be more convenient to consider the "VSC valve" to be not simply the IGBT elements that perform the switching, but also the distributed DC capacitors. In effect, such a valve is no longer simply a switch but is now a controllable voltage source, connected between the AC terminal of the corresponding phase unit, and one of the DC terminals (see Figure A.8).

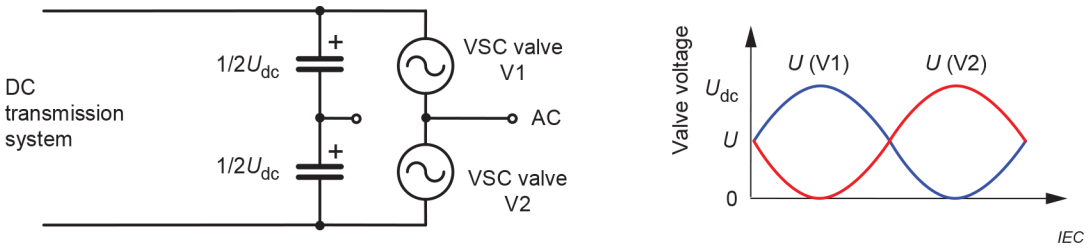


Figure A.8 – A single VSC phase unit with controllable voltage source type VSC valves

Each of the valves V1 and V2 in the phase unit produces an output voltage consisting of a sinusoidal AC component with a DC offset (equal to ½ U_{dc}). The output voltages of the two valves are varied such that at any given time, U(V1) + U(V2) = U_{dc}.

In principle, there can be many different methods of implementing such a valve, but two (closely related) methods have found widespread application: the modular multi-level converter (MMC) and the cascaded two-level converter (CTL).

A.5.2 Modular multi-level converter (MMC)

One implementation of the MMC circuit is shown in Figure A.9. The circuit of each submodule is modular, each submodule comprising a single, isolated DC capacitor and two IGBT switches. In effect, this circuit is very similar to that of the basic 2-level converter (see Figure A.4) except that the interconnections between submodules are made from the AC terminal (between IGBT1 and IGBT2) of one submodule, to one of the DC terminals of the neighbouring submodule. With this circuit, each submodule can produce two discrete output states: U = 0 (obtained by switching IGBT2 on) or U = $U_{dc\_submodule}$ (obtained by switching IGBT1 on). $U_{dc\_submodule}$ is the DC link voltage of a single submodule, which is much less than U_{dc}, the DC link voltage of the complete system.

With this circuit, it is possible to synthesize a unipolar valve output voltage with a maximum of U = U_{dc} and a minimum of U = 0. However, in common with all the converter topologies discussed so far, the converter has no capacity to suppress the overcurrent which arises from a short-circuit between the DC terminals of the converter. This is because although the two IGBTs can be turned off very quickly, a conducting path always remains through the freewheel diode in parallel with IGBT2.

Another implementation of the MMC circuit addresses this shortcoming by using a full-bridge arrangement, as shown on Figure A.10, instead of the half-bridge arrangement shown in Figure A.9.

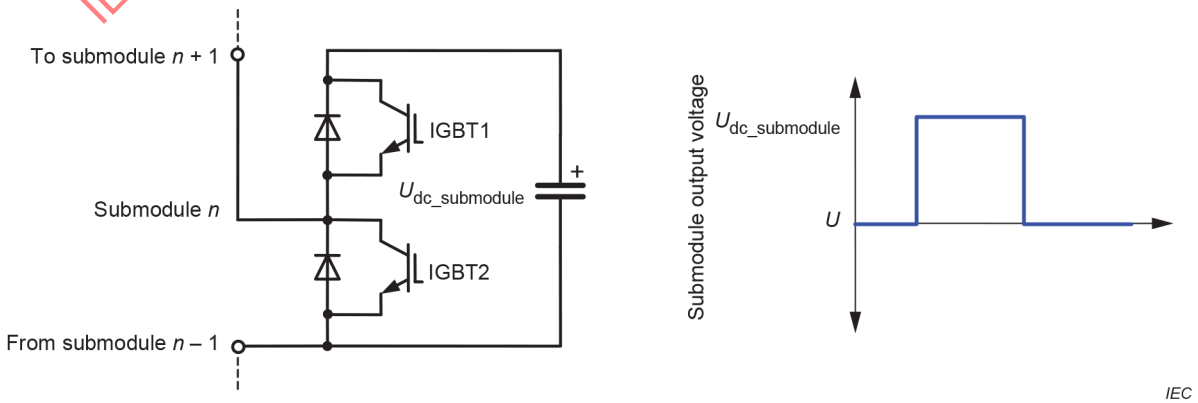


Figure A.9 – The half-bridge MMC circuit

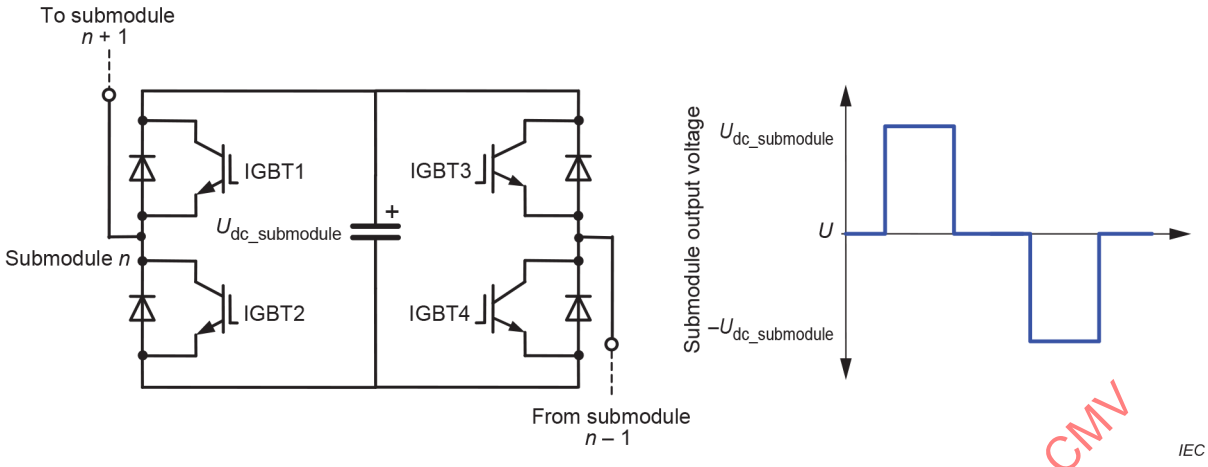


Figure A.10 – The full-bridge MMC circuit

In the full-bridge version of the MMC, each submodule contains four IGBTs instead of two, and can produce three discrete output voltage states:

- U = 0 (obtained by switching on either IGBT1 + IGBT3 or IGBT2 + IGBT4);
- $U = +U_{dc\_submodule}$ (obtained by switching on IGBT1 + IGBT4); or
- $U = -U_{dc\_submodule}$ (obtained by switching on IGBT2 + IGBT3).

The full-bridge circuit allows the valve to synthesize an output voltage of either polarity, allowing a new voltage-sourced converter to be connected as a tap to an existing HVDC line. Even when used on a unipolar DC line, the additional flexibility provided by the circuit allows the AC component of valve voltage to exceed the DC component (which is not possible with the half-bridge circuit), resulting in a lower AC current in the valve. In addition, the ability to suppress fault currents arising from short-circuits between the DC terminals can allow some simplification of protective functions. On the other hand the IGBT component count and the conduction losses, are increased by nearly double compared with the half-bridge version.

Since the MMC circuit is inherently modular, it is relatively straightforward to obtain high numbers of output levels, without requiring either PWM (which leads to higher switching losses and requires filtering) or series connected IGBTs (which leads to problems of ensuring voltage distribution). Industry standard IGBT devices can be used, which is not the case for valves of the switch type. Redundancy cannot be provided within each submodule (because the correct operation of the submodule requires both IGBTs to be healthy) and is usually provided by equipping the valve with a few extra submodules and ensuring that the entire submodule is shorted out in the event of a failure.

On the other hand, the number and size of discrete DC capacitors required can be considerable, and there may be difficulties in ensuring that all DC capacitor voltages remain balanced. In comparison with two- or three-level converters, therefore, this topology allows for a simpler valve design and lower losses at the expense of a more complex controls architecture and greater space requirement.

A.5.3 Cascaded two-level converter (CTL)

An advantage of the MMC circuit is that it avoids the need for IGBTs to be directly connected and switched synchronously in series. However, it is also possible to realise the MMC circuit with more than one IGBT in series in each switching position. Converters designed in this way are referred to as cascaded two-level converters in order to distinguish them from the MMC circuit, although in nearly every respect the circuit functions in exactly the same way as the MMC circuit.

In common with the MMC circuit, the CTL circuit can exist in half-bridge and full-bridge variants. The building-block of the CTL valve is referred to as a "cell" and the half-bridge version of a cell is shown on Figure A.11. Each of the two switch positions consists of n IGBTs in series, switched synchronously, and the cell DC capacitor will operate at approximately n times the voltage of a submodule DC capacitor in the MMC circuit.

In operational terms the only significant difference between the CTL and MMC circuits is that the CTL circuit produces a valve output voltage containing fewer, larger, steps than the MMC circuit. Its harmonic performance is therefore not quite as good as that of the MMC circuit, although if the number of IGBTs per switching position is modest (for example, 5 to 10) then it can still achieve very high waveform quality while permitting some simplification of the control system compared to the MMC circuit. The CTL circuit does, however, require sophisticated IGBT gate drive circuits and a more specialised type of IGBT, in common with all valves of the switch type.

Redundancy is provided within each cell by equipping each switch position with more IGBTs than are normally required to operate within the rated voltage of the converter.

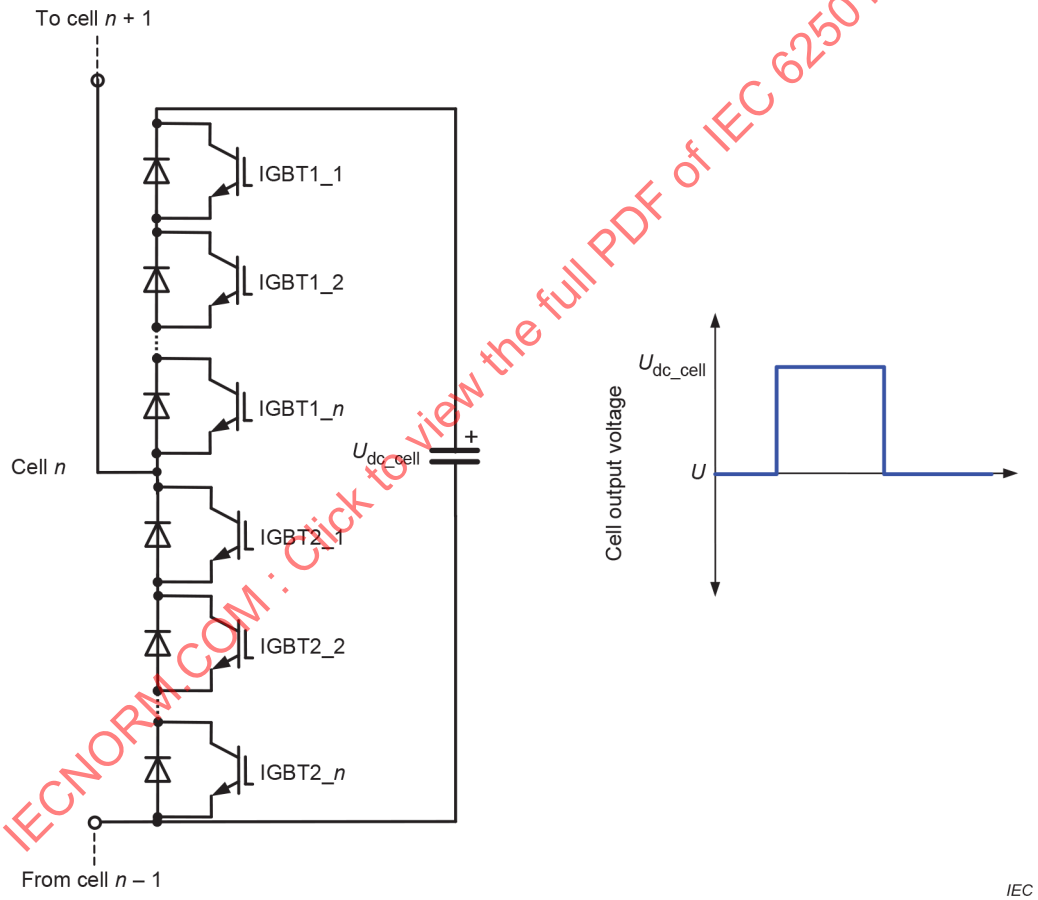


Figure A.11 – The half-bridge CTL circuit

A.5.4 Terminology for valves of the controllable voltage source type

Figure A.12 and Figure A.13 illustrate the main constructional terms for valves of the MMC and CTL type respectively, to explain the meaning of terms such as VSC level, submodule and cell.

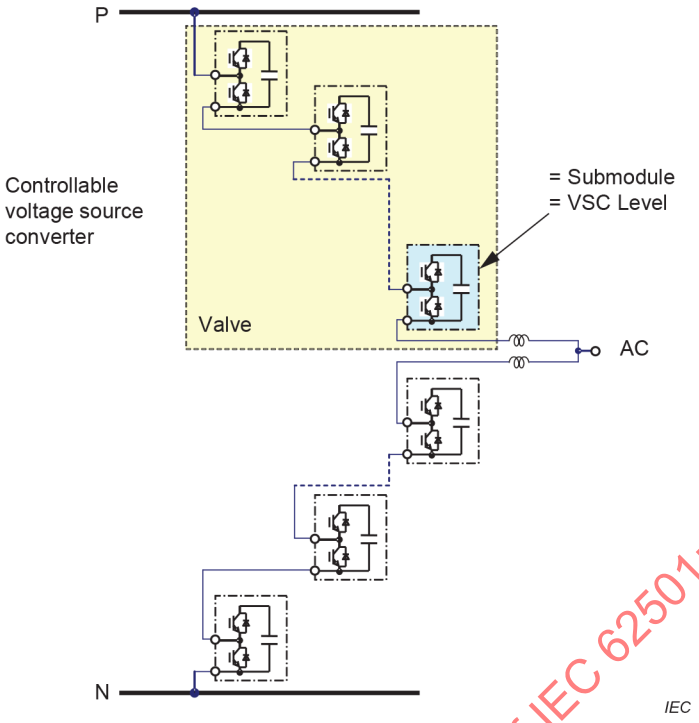


Figure A.12 – Construction terms in MMC valves

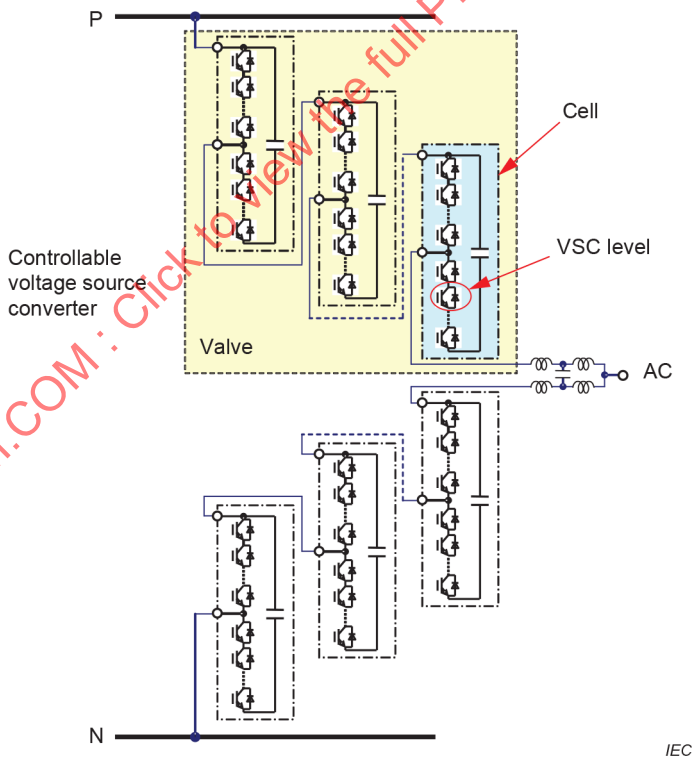


Figure A.13 – Construction terms in CTL valves

A.6 Hybrid VSC valves

Some published literature has suggested alternative types of VSC valve which possess characteristics of both the switch type and controllable voltage source type. Since the pace of development in this field is quite rapid it is considered beyond the scope of this document to present a detailed treatment of these new converter topologies; however, a basic treatment is given in CIGRE Technical Brochure No. 492.

A.7 Main differences between VSC and conventional HVDC valves

VSC valves differ from conventional thyristor-based HVDC valves in many respects. It is important to appreciate these differences in order to understand the differences in approach that need to be taken when testing such valves.

Whilst there are a great many differences, the principal ones that affect valve testing are as follows.

- VSC valves are capable of both being turned ON and being turned OFF by control action. In contrast, conventional HVDC thyristor valves can only be turned ON by control action and, to achieve turn OFF, require the external circuit to force the current to zero and then apply a period of reverse voltage. Hence, tests to demonstrate minimum extinction angles or positive voltage transients during the recovery interval (which are so important for thyristor valves), have no significance for VSC valves.
- In most VSC valves, the valve is not capable of supporting reverse voltage (because it contains in-built freewheel diodes), but can conduct reverse current. In conventional HVDC thyristor valves, the valve can withstand reverse voltage but not conduct reverse current.
- In VSC valves, protective turn-ON is generally not used because of the risk of creating a short-circuit across the DC capacitor, but instead protective turn-OFF is employed as a means of suppressing overcurrents. By contrast, in conventional HVDC thyristor valves, protective turn-ON is widely used and protective turn-OFF is not possible.
- The large DC-side capacitance means that there are few circumstances where a VSC phase unit can experience fast voltage transients between terminals. In valves of the "controllable voltage source" type (where some of the DC capacitance is embedded within the valve) the same is also true for voltages between the terminals of the valve.

Annex B
(informative)

Valve component fault tolerance

Fault tolerance capability may be defined as the ability of an HVDC VSC valve to perform its intended function, until a scheduled shutdown, with faulted components or subsystems or overloaded components, and not lead to any unacceptable failure of other components, or extension of the damage due to the faulted condition. Special features may be required in the design to ensure fault tolerance.

Tests to demonstrate the valve component fault tolerance are not categorized as type tests since most of them are destructive tests of valve or valve components and the tests are usually done on small number of valve levels. Those tests should be done in design stage of new type of valves for compliance check of valve fault component tolerance. Supplier should document the tests and provide project related report, based on experience in lieu, on purchasers' request.

Examples of faults for which fault tolerance may be required are given below:

a) Failure of an IGBT or diode

   Even though a short-circuit IGBT-diode pair or the operation of an external valve level shorting device will shunt the other components at the valve level, in some designs there may be a danger of overload of current connections or changes in clamping load.

b) Missing of on-gate at one valve level due to loss of normal on-gate pulses to that level

   Missing of on-gate leads to parallel overvoltage of the components at the affected level.

c) Insulation failure of a snubber capacitor, snubber resistor or other components if applicable

   Insulation failure of any component in parallel with the IGBTs or diodes can attract load current into it, leading to a hazardous condition.

d) Leakage of small quantities of valve coolant

   If the valve is liquid cooled, small leaks may not be easily detected. Escaped coolant can contaminate sensitive components, leading to malfunction, and can increase the probability of insulation failure. However, experience acquired in the wet test performed on both LCC and VSC valves indicates that the valve wet test on a new and dust free valve surface is unable to identify locations where might cause valve dielectric failure in service due to the leakage of small quantities of valve coolant. IEEE Std 857™-1996, *IEEE Recommended Practice for Test Procedures for High-Voltage Direct-Current Thyristor Valves*, to which the wet test is often referred, was withdrawn in 2010.

e) Submodule / Cell internal short-circuit current

   Either misfiring of IGBT, short-circuit of IGBT-diode pair or insulation failure may lead to an internal capacitor discharge current. Under these short-circuit conditions, the fault should be self-contained without impacting the normal operation of adjacent submodule / cell. In particular, the fault should not lead to a flashover outside the affected submodule / cell, damage leading to mal-operation caused by projected debris or electromagnetic interference on neighbouring submodule / cell. Any visible light escaping from the faulted submodule / cell should not cause fire or arc detection systems in the valve hall to shut down the converter.

f) Submodule / Cell external short-circuit current

Similarly to case (e) above, if a short-circuit takes place between the external terminals of the submodule / cell, or across several submodule / cell (for example between tiers of a valve stack) then the capacitors of the submodule / cell(s) that were in the output state at the time of the short circuit, will discharge their capacitors into the short-circuit. Although the rate of change of current is lower than for case (e) because of the larger loop inductance, it is still very high and can lead to a severe rate of change of magnetic field, potentially affecting nearby electronic circuits. Depending on the design philosophy adopted for the valve, tests may be needed to demonstrate that the IGBTs will safely turn off before the capacitors can fully discharge and that the resulting electromagnetic disturbance does not cause mal-operation of nearby electronic circuits.

g) Effects of fast transient overvoltages on electronics

Certain events such as lightning strikes on the AC or DC systems close to the converter station, switching actions of the valves (including protective blocking) and bushing flashovers inside the valve hall may lead to fast transient overvoltages which, although not necessarily of an amplitude sufficient to pose a risk of insulation failure, could subject the electronic boards in the valve to a very high dv/dt. Depending on the design philosophy of the overall converter station for such faults, tests may be necessary to demonstrate that the electronic boards continue in operation without damage or malfunction under such conditions.

The purchaser should review the design offered with the supplier to determine the probability and likely consequences of certain failures. Where appropriate, consideration should be given, to the performance of special tests to verify critical aspects of the fault tolerance capability of the valve. The details of such tests are subject to agreement on a case-by-case basis.

Annex C
(informative)

Valve losses determination

As transmission losses are directly related to the investment and operational costs, they are one of the most important factors for high voltage direct current (HVDC) project evaluation. For voltage sourced converters (VSC), valve losses are the largest part of the total converter station losses and therefore the determination and evaluation of the VSC valve losses becomes highly important.

Presently, the losses of VSC valves are determined based on the calculation methods of IEC 62751-1 and IEC 62571-2. The calculation method requires detailed information such as the parameters of semiconductor devices, VSC valve design characteristics and operating modes, which are usually not directly available to the HVDC system purchaser/user, who consequently finds it difficult to evaluate the calculated losses results.

Therefore, CIGRE working group B4.75 was set up in 2017 to perform a feasibility study to assess laboratory loss measurement methods on VSC valves for loss calculation evaluation purposes and to make recommendations considering the pros and cons of such measurement methods versus the methods in IEC 62751. The results of this working group were published in 2021 as CIGRE TB 844: "Feasibility study for assessment of lab losses measurement of VSC valves".

The brochure starts with a general description of losses in VSC HVDC converter valves, the origins of different losses in components, the dependency of the losses on different operating modes, as well as special aspects of different designs. This is followed by a summary of the current practice for valve losses determination, including the modelling of the semiconductor parameters and then by a discussion on how the transparency of the overall calculation process can be enhanced. As the main study results of the WG B4.75, an evaluation of the existing methods to measure losses is provided. This is complemented by an overview of the operation conditions and additional aspects for losses measurement (such as commercial aspects) that need to be taken into account. In the last part, the results are summarized and recommendations for application of losses measurement are given, which can be used as guidance for the introduction of losses measurements in the operational type tests of VSC valves.

The conclusion of CIGRE TB 844 is that the laboratory measurement of valve losses is feasible, although the level of accuracy achievable is still quite poor. The general recommendation therefore is that the laboratory measurement should become a standard part of the operational type tests of the VSC valves, such that in the coming years greater industry experience can be gained in this area. However, it is not recommended that the measured valve losses are used as part of the financial evaluation criteria for the HVDC project, until there is a good industry experience and consensus over what should be a realistically achievable level of measurement uncertainty.

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IEC 60146-2, *Semiconductor converters – Part 2: Self-commutated semiconductor converters including direct d.c. converters*

IEC 61975, *High-voltage direct current (HVDC) installations – System tests*

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IEC 62751-1, *Power losses in voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) systems – Part 1: General requirements*

IEEE Std 857™-1996, *IEEE Recommended Practice for Test Procedures for High-Voltage Direct-Current Thyristor Valves*

CIGRE Technical Brochure No. 269, *VSC Transmission*

CIGRE Technical Brochure No. 447, *Components Testing of VSC Systems for HVDC Applications*

CIGRE Technical Brochure No. 492, *Voltage Sourced Converter (VSC) for HVDC Power Transmission – Economic Aspects and Comparison with other AC and DC Technologies*

CIGRE Technical Brochure No. 844, *Feasibility study for assessment of lab losses measurement of VSC valves*

SOMMAIRE

COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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VALVES À CONVERTISSEUR DE SOURCE DE TENSION (VSC) POUR LE TRANSPORT D'ÉNERGIE EN COURANT CONTINU À HAUTE TENSION (CCHT) – ESSAIS ÉLECTRIQUES

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Cette deuxième édition annule et remplace la première édition parue en 2009, son Amendement 1:2014 et son Amendement 2:2017. Cette édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) un nouveau tableau relatif aux conditions d'utilisation de la substitution de preuve (Tableau 1) a été inséré;

b) les paramètres d'essai relatifs à l'essai de support de valve sous tension continue (7.3.2) et à l'essai de MVU sous tension continue (8.4.1) ont été mis à jour;

c) l'Article 9 concernant l'essai sous tension alternative-continue entre les bornes de valve a été réorganisé et des variantes ont été ajoutées en 9.4.2 pour les essais individuels sous tension alternative et continue;

d) l'essai de décharge partielle a été supprimé du programme des essais individuels de série;

e) des informations complémentaires relatives à la tolérance aux pannes des composants de valve ont été ajoutées à l'Annexe B;

f) la détermination des pertes de valve a été ajoutée à l'Annexe C.

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
22F/731/CDV	22F/748A/RVC

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

Ce document a été rédigé selon les Directives ISO/IEC, Partie 2, il a été développé selon les Directives ISO/IEC, Partie 1 et les Directives ISO/IEC, Supplément IEC, disponibles sous www.iec.ch/members_experts/refdocs. Les principaux types de documents développés par l'IEC sont décrits plus en détail sous www.iec.ch/publications/.

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VALVES À CONVERTISSEUR DE SOURCE DE TENSION (VSC) POUR LE TRANSPORT D'ÉNERGIE EN COURANT CONTINU À HAUTE TENSION (CCHT) – ESSAIS ÉLECTRIQUES

1 Domaine d'application

La présente Norme internationale s'applique aux valves à convertisseur auto-commuté, conçues pour être utilisées dans un convertisseur de source de tension (VSC) en pont triphasé pour le transport d'énergie en courant continu à haute tension ou dans une liaison dos-à-dos, ainsi qu'aux valves à freinage dynamique. Elle est limitée aux essais de type électriques et de série.

Le présent document peut servir de guide pour les essais des valves à VSC à haute tension utilisées dans les systèmes de stockage d'énergie (ESS).

Les essais spécifiés dans le présent document sont basés sur des valves isolées par l'air. Les exigences d'essai et les critères d'acceptation peuvent servir de guide pour spécifier les essais de type électriques et de série d'autres types de valves.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

IEC 60060 (toutes les parties), *Techniques des essais à haute tension*

IEC 60071 (toutes les parties), *Coordination de l'isolement*

IEC 60270, *Techniques des essais à haute tension – Mesures des décharges partielles*

IEC 60700-1:2015, *Valves à thyristors pour le transport d'énergie en courant continu à haute tension (CCHT) - Partie 1: Essais électriques*
IEC 60700-1:2015/AMD1:2021

IEC 62747, *Terminologie relative aux convertisseurs de source de tension (VSC) des systèmes en courant continu à haute tension (CCHT)*

ISO/IEC 17025, *Exigences générales concernant la compétence des laboratoires d'étalonnages et d'essais*

3 Termes et définitions

Pour les besoins du présent document, les termes et les définitions de l'IEC 62747 ainsi que les suivants s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse https://www.electropedia.org/
- ISO Online browsing platform: disponible à l'adresse https://www.iso.org/obp

3.1 Termes relatifs à la coordination de l'isolement

3.1.1
tension de tenue d'essai
valeur d'une tension d'essai de forme d'onde normalisée pour laquelle une nouvelle valve, dont l'intégrité est intacte, ne présente aucune décharge disruptive et respecte tous les autres critères d'acceptation spécifiés pour l'essai particulier, lorsqu'elle est soumise à un nombre spécifié d'applications ou à une durée spécifiée d'application de la tension d'essai, dans les conditions spécifiées

3.1.2
isolement interne
air extérieur aux composants et matériaux isolants de la valve mais contenu dans le profil de la valve ou de l'ensemble à valves multiples

3.1.3
isolement externe
air situé entre la surface externe de la valve ou de l'ensemble à valves multiples et son environnement

3.2 Termes relatifs aux semiconducteurs de puissance

3.2.1
dispositif à semiconducteur blocable
dispositif à semiconducteur commandable qui peut être réactivé et coupé par un signal de commande, IGBT, par exemple

Note 1 à l'article: Il existe plusieurs types de dispositifs à semiconducteur blocable qui peuvent être utilisés dans les convertisseurs VSC pour des applications CCHT. Pour des raisons pratiques, le terme IGBT est utilisé tout au long de la présente norme pour faire référence au principal dispositif à semiconducteur blocable. Cependant, la norme s'applique également aux autres types de dispositifs à semiconducteur blocable.

3.2.2
transistor bipolaire à grille isolée
IGBT
dispositif à semiconducteur blocable possédant trois bornes: une borne de grille (G) et deux bornes de charge: émetteur (E) et collecteur (C)

Note 1 à l'article: En appliquant des tensions appropriées entre la grille et l'émetteur, le courant de charge peut être commandé, c'est-à-dire qu'il peut être établi ou coupé.

Note 2 à l'article: L'abréviation "IGBT" est dérivée du terme anglais développé correspondant "insulated gate bipolar transistor".

3.2.3
diode de roue libre
DRL
dispositif à semiconducteur de puissance ayant les caractéristiques d'une diode

Note 1 à l'article: Une DRL possède deux bornes: une anode (A) et une cathode (K). Le courant dans les DRL circule en sens opposé au courant de l'IGBT.

Note 2 à l'article: Les DRL sont caractérisées par leur capacité à faire face à des taux élevés de chute de courant dus au comportement de commutation de l'IGBT.

3.2.4
paire IGBT-diode
combinaison de l'IGBT et de la DRL connectés en parallèle en sens inverse

3.3 États de fonctionnement du convertisseur

3.3.1
état bloqué
condition du convertisseur dans laquelle un signal de fermeture est appliqué en continu à tous les IGBT du convertisseur

Note 1 à l'article: Généralement, le convertisseur est à l'état bloqué après la mise sous tension.

3.3.2
état débloqué
condition du convertisseur dans laquelle des signaux d'ouverture et de fermeture sont appliqués de manière répétitive aux IGBT du convertisseur

3.3.3
blocage de protection de la valve
dispositif de protection de la valve ou du convertisseur d'une contrainte électrique excessive par la fermeture d'urgence de tous les IGBT dans une ou plusieurs valves

3.3.4
niveau de palier de tension
échelon de tension dû à la commutation d'une valve ou d'une partie d'une valve pendant l'état débloqué du convertisseur

Note 1 à l'article: Pour les valves de type à source de tension commandable, le niveau de palier de tension correspond à la variation de tension due à la commutation d'un sous-module ou d'une cellule. Pour les valves de type commutateur, le niveau de palier de tension correspond à la variation de tension due à la commutation de la valve complète.

Note 2 à l'article: L'Annexe A fournit une vue d'ensemble des convertisseurs VSC utilisés pour le transport d'énergie CCHT.

3.4 Termes relatifs à la construction des VSC

3.4.1
unité de phase VSC
équipement utilisé pour raccorder les deux barres omnibus de courant continu à une borne de courant alternatif

3.4.2
valve à VSC de type commutateur
combinaison de paires IGBT-diode connectées en série et configurées de manière à être commutées simultanément en une unité fonctionnelle simple

3.4.3
valve à VSC de type à source de tension commandable
ensemble complet à source de tension commandable, généralement connecté entre une borne de courant alternatif et une borne de courant continu

3.4.4
valve à diode
valve à semiconducteur contenant uniquement des diodes comme principaux dispositifs à semiconducteur, pouvant servir dans certaines topologies de VSC

3.4.5
valve à freinage dynamique
dispositif commandable complet qui sert à réguler l'absorption d'énergie dans la résistance de freinage ou autres composants

3.4.6
valve
valve à VSC, valve à freinage dynamique ou valve à diode, selon le contexte

3.4.7
sous-module
partie d'une valve à VSC comprenant des commutateurs et des diodes commandables connectés en demi-pont ou en pont complet, ainsi que leurs auxiliaires immédiats et condensateurs de stockage, le cas échéant, où chaque commutateur commandable comporte un seul dispositif à valve commuté connecté en série

3.4.8
cellule
bloc module MMC dans lequel chaque position de commutateur est composée de plusieurs paires IGBT-diode connectées en série

Note 1 à l'article: Voir Figure A.13.

3.4.9
niveau de valve à VSC
plus petite unité fonctionnelle indivisible d'une valve à VSC

Note 1 à l'article: Pour toute valve à VSC dans laquelle les IGBT sont connectés en série et manœuvrés simultanément, un niveau de valve à VSC correspond à une paire IGBT-diode, y compris ses auxiliaires (voir Figure A.13). Pour un type MMC sans paires IGBT-diode connectées en série, un niveau de valve correspond à un sous-module associé à ses auxiliaires (voir Figure A.12).

3.4.10
niveau de valve à diode
partie d'une valve à diode composée d'une diode et des circuits et composants associés, le cas échéant

3.4.11
niveaux redondants
nombre maximal de niveaux de valve à VSC connectés en série ou de niveaux de valve à diode dans une valve, qui peut être court-circuité par un ordre externe ou interne sans que le fonctionnement sécurisé de la valve en soit altéré, comme il est démontré par les essais de type, et qui, en cas de dépassement, exige l'arrêt de la valve pour permettre le remplacement des niveaux défaillants ou l'acceptation d'un risque accru de dysfonctionnements

Note 1 à l'article: Dans les conceptions de valves telles que le convertisseur à deux niveaux monté en cascade, qui contiennent deux chemins de conduction ou plus dans chaque cellule et comportent des niveaux de valve à VSC connectés en série dans chaque chemin, les niveaux redondants doivent être comptés uniquement dans un chemin de conduction de chaque cellule.

3.4.12
niveau de valve à freinage dynamique
partie d'une valve à freinage dynamique comprenant un commutateur commandable et une diode associée, ou des commutateurs et des diodes commandables connectés en parallèle, ou des commutateurs et des diodes commandables connectés en pont, ainsi que leurs auxiliaires immédiats, condensateurs de stockage et résistances de dissipation d'énergie, le cas échéant

3.5 Termes relatifs à la structure des valves

3.5.1
structure de valve
composants de structure d'une valve, exigés afin de soutenir physiquement les modules de valve

3.5.2
support de valve
partie de la valve fournissant un support mécanique et l'isolation électrique de la terre à la partie sous tension de la valve

3.5.3
ensemble à valves multiples
MVU
disposition mécanique comportant au moins deux valves ou une ou plusieurs unités de phase à VSC partageant un support de valve commun

Note 1 à l'article: Toutes les topologies et la disposition physique des convertisseurs peuvent ne pas contenir de MVU.

Note 2 à l'article: L'abréviation "MVU" est dérivée du terme anglais développé correspondant "multiple valve unit".

3.5.4
section de valve
assemblage électrique défini à des fins d'essais, comportant un certain nombre de niveaux de valve et d'autres composants, et présentant les propriétés électriques préassignées d'une valve complète

Note 1 à l'article: Pour les valves du type à source de tension commandable, la section de valve doit inclure le condensateur à courant continu de cellule ou de sous-module en plus des niveaux de valve à VSC.

Note 2 à l'article: Le nombre minimal de niveaux de valve à VSC ou à diode autorisé dans une section de valve est défini avec les exigences de chaque essai.

4 Exigences générales

4.1 Lignes directrices concernant la réalisation d'essais de type

4.1.1 Substitution de preuve

Chaque conception de valve doit être soumise aux essais de type spécifiés dans le présent document. S'il est possible de démontrer que la valve est similaire à une valve précédemment soumise à essai, au lieu de réaliser un essai de type ou des parties individuelles de cet essai, le fournisseur peut soumettre à l'acheteur, pour examen, le rapport d'essai d'un essai de type précédent. Il convient de l'accompagner d'un rapport distinct détaillant les différences de conception et démontrant la manière dont l'essai de type référencé satisfait aux objectifs de l'essai pour la conception proposée. Les conditions d'utilisation de la substitution de preuve sont énumérées dans le Tableau 1.

Tableau 1 – Conditions d'utilisation de la substitution de preuve issue d'un autre projet CCHT

Essai de type	Paragraphe	Conditions
Essais de fonctionnement	6	• Niveaux de valve à soumettre à essai inférieurs en nombre ou identiques • Même conception des niveaux de valve • Même conception de l'électronique de valve • Contrainte de tension et contrainte thermique identiques ou inférieures [a] sur chaque niveau de valve
Essais diélectriques sur la structure de support de valve	7	• Structure de valve identique, y compris les tuyaux de refroidissement, les chemins de câble et le système de mise à la terre, le cas échéant • Même matériau de valve et même dimension géométrique • Distance d'isolement supérieure ou égale par rapport à la salle des valves et aux autres équipements associés à l'intérieur de la salle des valves • Contrainte de tension inférieure ou égale, y compris la contrainte de tension continue, la contrainte de tension alternative et les contraintes de tension de choc
Essais diélectriques sur un ensemble à valves multiples	8	• Même géométrie de MVU entre les valves
Essais diélectriques entre les bornes de valve	9	• Structure de valve identique, y compris les tuyaux de refroidissement, les chemins de câble et le système de mise à la terre, le cas échéant • Même matériau de valve et même dimension géométrique • Contrainte de tension inférieure ou égale
Essai de blocage de l'IGBT en cas de surintensité	10	• Même conception des niveaux de valve • Même conception de l'électronique de valve • Contrainte de courant présumé identique ou inférieure
Essai de courant de court-circuit	11	• Même conception des niveaux de valve • Mêmes composants de mise en court-circuit, s'il existe, et même fonction • Même conception de l'électronique de valve • Contrainte de courant de court-circuit identique ou inférieure
Essais d'insensibilité de la valve aux perturbations électromagnétiques	12	• Identiques à celles indiquées dans les Articles 6 et 9

[a] La contrainte thermique des dispositifs à semiconducteur est un effet combiné du courant et du refroidissement. La contrainte thermique du dispositif est caractérisée par la température de jonction dudit dispositif.

4.1.2 Choix de l'objet d'essai

Le présent paragraphe ne s'applique pas aux essais réalisés sur la structure de support de la valve et sur l'ensemble à valves multiples. L'objet d'essai pour ces essais est défini en 7.2 et 8.3.

a) Les essais de type peuvent être réalisés soit sur une valve ou un MVU complet, soit sur leurs parties, comme indiqué dans le Tableau 4.

b) Le nombre minimal de niveaux de valve à soumettre à l'essai de type fonctionnel, en fonction des niveaux de valve dans une valve unique, est tel qu'indiqué dans le Tableau 2. Ce nombre s'applique aux essais de type des Articles 6, 10, 11 et 12. Ces niveaux de valve doivent être soumis à essai dans un ou plusieurs montages d'essai sur plusieurs sections de valve telles que définies dans ces articles.

Tableau 2 – Nombre minimal de niveaux de valve à soumettre à l'essai de type fonctionnel en fonction du nombre de niveaux de valve par valve

Nombre de niveaux de valve, y compris le niveau redondant par valve	Nombre total de niveaux de valve à soumettre à essai
1 à 50	Nombre de niveaux de valve dans une valve
51 à 250	50
≥ 251	20 %

Le nombre minimal de niveaux de valve à soumettre à l'essai de type diélectrique peut être inférieur ou égal au nombre spécifié pour l'essai de type fonctionnel.

Le nombre minimal de niveaux de valve doit toutefois être représentatif de la conception diélectrique de la valve.

c) Il est généralement recommandé d'utiliser les mêmes sections de valve pour tous les essais de type. Cependant, différents essais peuvent être réalisés sur différentes sections de valve en parallèle, afin d'accélérer le programme d'exécution des essais.

d) Avant le début des essais de type, la résistance de la valve, des sections et/ou des composants de valve aux essais de production doit être démontrée afin d'assurer une fabrication appropriée.

4.1.3 Procédure d'essai

Les essais doivent être effectués conformément à l'IEC 60060, le cas échéant en tenant dûment compte de l'IEC 60071 (toutes les parties). Les mesures de décharge partielle doivent être réalisées conformément à l'IEC 60270.

4.1.4 Température ambiante pour les essais

Les essais doivent être effectués à la température ambiante prédominante de l'installation d'essai, sauf spécification contraire.

4.1.5 Fréquence des essais

Les essais diélectriques en courant alternatif peuvent être réalisés soit à 50 Hz, soit à 60 Hz. Les essais de fonctionnement doivent être effectués à la fréquence de service.

4.1.6 Rapports d'essai

À l'issue des essais de type, le fournisseur doit produire des rapports d'essais de type conformément à l'Article 15.

4.1.7 Conditions à prendre en compte pour la détermination des paramètres des essais de type

Les paramètres des essais de type doivent être déterminés sur la base des conditions de fonctionnement et de défaut les plus défavorables auxquelles la valve peut être soumise, conformément aux études du système. La Brochure technique nº 447 du CIGRE fournit des recommandations concernant les conditions.

4.2 Facteur de correction atmosphérique

Lorsque l'article correspondant le spécifie, une correction atmosphérique doit être appliquée aux tensions d'essai conformément à l'IEC 60060-1. Les conditions de référence auxquelles les corrections doivent être apportées sont les suivantes:

– pression:

- si la coordination de l'isolement de la partie soumise à essai de la valve est fondée sur les tensions de tenue assignées normalisées conformes à l'IEC 60071-1, les facteurs de correction sont uniquement appliqués aux altitudes supérieures à 1 000 m. Ainsi, si l'altitude du site a_s sur lequel le matériel est installé est ≤ 1 000 m, la pression d'air atmosphérique normale (b_0 = 101,3 kPa) doit alors être utilisée sans correction de l'altitude; si a_s >1 000 m, la procédure normalisée conforme à l'IEC 60060-1 est utilisée, mais la pression atmosphérique de référence b_0 est remplacée par la pression atmosphérique correspondant à une altitude de 1 000 m ($b_{1\ 000m}$);
- si la coordination de l'isolement de la partie soumise à essai de la valve n'est pas fondée sur les tensions de tenue assignées normalisées conformes à l'IEC 60071-1, la procédure normalisée conforme à l'IEC 60060-1 est utilisée avec la pression atmosphérique de référence b_0 (b_0 = 101,3 kPa);

– température: température de l'air maximale de conception de la salle des valves (°C);

– humidité: humidité absolue minimale de conception de la salle des valves (g/m^3).

Les combinaisons réalistes les plus défavorables de température et d'humidité qui peuvent exister dans la pratique doivent être utilisées pour la correction atmosphérique.

Les valeurs à utiliser doivent être spécifiées par le fournisseur.

4.3 Traitement de la redondance

4.3.1 Essais de fonctionnement

Pour les essais de fonctionnement, les niveaux de valve redondants ne doivent pas être court-circuités. Les tensions d'essai utilisées doivent être ajustées au moyen d'un facteur d'échelle k_n:

$$k_n = \frac{N_{tut}}{N_t - N_r}$$

où

N_{tut} est le nombre de niveaux de valve en série dans l'objet d'essai;

N_t est le nombre total de niveaux de valve en série dans la valve;

N_r est le nombre total de niveaux de valve redondants en série dans la valve.

4.3.2 Essais diélectriques

Pour tous les essais diélectriques entre les bornes de valves, les niveaux de valve redondants doivent être court-circuités. L'emplacement des niveaux de valve à court-circuiter doit faire l'objet d'un accord entre l'acheteur et le fournisseur.

NOTE En fonction de la conception, des limites peuvent être imposées au niveau de la répartition des niveaux de valve court-circuités. Par exemple, il peut exister une limite supérieure relative au nombre de niveaux de valve court-circuités dans une seule section de valve.

Pour tous les essais diélectriques sur une section de valve, les tensions d'essai utilisées doivent être ajustées au moyen d'un facteur d'échelle k_0:

$$k_0 = \frac{N_{tu}}{N_t - N_r}$$

où

N_{tu} est le nombre de niveaux de valve non court-circuités en série connectés dans l'objet d'essai;

N_t est le nombre total de niveaux de valve en série dans la valve;

N_r est le nombre total de niveaux de valve redondants en série dans la valve.

4.4 Critères de réussite des essais de type

4.4.1 Généralités

Même si le plus grand soin est apporté à la conception des valves, l'expérience des applications à semiconducteur montre qu'il est impossible d'éviter des défaillances aléatoires occasionnelles des composants de niveaux de valve pendant l'exploitation. Même si ces défaillances peuvent être liées à des contraintes, elles sont considérées comme aléatoires dans la mesure où leur cause ou la relation entre le taux de défaillance et la contrainte n'est pas prévisible ou ne peut être quantifiée de manière précise. Les essais de type soumettent, dans un délai très court, les valves ou sections de valve à plusieurs contraintes correspondant généralement aux pires contraintes auxquelles peut parfois être soumis le matériel pendant la durée de vie de la valve. De ce fait, les critères de réussite des essais de type définis ci-dessous n'autorisent qu'un nombre réduit de défaillances des niveaux de valve au cours des essais de type, à condition que ces défaillances soient rares et ne soient pas le révélateur d'une conception inappropriée et à condition que le niveau de valve défaillant permette au reste de la valve ou section de valve de continuer à fonctionner sans altérer la performance.

4.4.2 Critères applicables aux niveaux de valve

Les critères suivants sont applicables aux niveaux de valve.

a) Si, à la suite d'un essai de type répertorié à l'Article 5, plusieurs niveaux de valve (ou plus de 1 % des niveaux de valve soumis à essai, si cette valeur est supérieure) ont été court-circuités ou mis à circuit ouvert, la valve doit alors être considérée comme n'ayant pas satisfait aux essais de type.

b) Si, à la suite d'un essai de type, un niveau de valve (ou plus si la valeur s'inscrit dans une limite de 1 %) a été court-circuité ou mis à circuit ouvert, le ou les niveaux défaillants doivent alors être rétablis et cet essai de type répété.

c) Si le nombre cumulé des niveaux de valve court-circuités ou à circuit ouvert au cours de tous les essais de type dépasse 3 % des niveaux de valve soumis à essai, la valve doit alors être considérée comme n'ayant pas satisfait aux essais de type.

d) La valve ou les sections de valve doivent être vérifiées après chaque essai de type afin de déterminer si des niveaux de valve ont été court-circuités ou mis à circuit ouvert. Avant de poursuivre les essais, les paires IGBT-diode ou les composants auxiliaires qui se sont révélés défaillants au cours ou à la fin d'un essai de type peuvent être remplacés.

e) À l'issue du programme d'essais, la valve ou les sections de valve doivent faire l'objet d'une série d'essais de vérification, qui doivent inclure au minimum:

   – la vérification de la tenue en tension des niveaux de valve;
   – la vérification des circuits de déclenchement;
   – la vérification des circuits de surveillance;
   – la vérification des circuits de protection faisant partie intégrante de la valve;
   – la vérification des circuits de répartition des potentiels.

f) Les courts-circuits des niveaux de valve survenant au cours des essais de vérification doivent être décomptés en tant que partie des critères d'acceptation définis ci-dessus. En plus des niveaux court-circuités ou mis à circuit ouvert, le nombre total de niveaux de valve présentant des défauts n'occasionnant pas de court-circuit de niveaux de valve, qui sont découverts au cours du programme d'essais de type et de l'essai de vérification ultérieur, ne doit pas dépasser 3 % du nombre de niveaux de valve soumis à essai lors des essais de type diélectrique et de fonctionnement. Si le nombre de ces niveaux dépasse 3 %, la nature des défauts et leur cause doivent être revues et une action supplémentaire, s'il y a lieu, doit faire l'objet d'un accord entre l'acheteur et le fournisseur.

g) Lorsque les critères de pourcentage sont appliqués pour déterminer le nombre maximal autorisé de niveaux de valve court-circuités ou mis à circuit ouvert ainsi que le nombre maximal autorisé de niveaux avec des défauts n'ayant pas occasionné de court-circuit de niveaux de valve, il est courant d'arrondir toutes les fractions au nombre entier supérieur, comme représenté dans le Tableau 3.

Tableau 3 – Défauts de niveaux de valve autorisés au cours des essais de type

Nombre de niveaux de valve soumis à essai	Nombre de niveaux de valve qu'il est permis de court-circuiter ou de mettre à circuit ouvert dans un essai de type quelconque	Nombre total de niveaux de valve qu'il est permis de court-circuiter ou de mettre à circuit ouvert dans un essai de type quelconque	Nombre supplémentaire de niveaux de valve, dans tous les essais de type, ayant fait l'objet d'un défaut mais n'ayant pas été court-circuités ou mis à circuit ouvert
Jusqu'à 33	1	1	1
34 à 67	1	2	2
68 à 100	1	3	3
101 à 133	2	4	4

La répartition de niveaux court-circuités ou mis à circuit ouvert et d'autres défauts de niveaux de valve à l'issue de tous les essais de type doit être essentiellement aléatoire et ne doit présenter aucun signe indiquant une conception inappropriée.

4.4.3 Critères applicables à la valve dans son ensemble

Une défaillance ou un claquage externe sur un matériel électrique commun associé à plusieurs niveaux de valve de la valve, ou une décharge disruptive dans le matériau diélectrique faisant partie de la structure de la valve, des conduits de refroidissement, des conduits de lumière ou d'autres parties isolantes du système de transmission et de répartition des impulsions, ne doit pas être autorisé.

Les températures de surface des composants et des conducteurs, ainsi que les jonctions et connexions associées acheminant du courant, et la température des surfaces de montage adjacentes doivent toujours rester dans les limites autorisées par la conception.

5 Liste des essais de type

Le Tableau 4 dresse la liste des essais de type présentés dans les Articles 6, 7, 8, 9, 10, 11 et 12.

Tableau 4 – Liste des essais de type

Essai de type	Article ou paragraphe	Objet d'essai
Essai en service permanent maximal	6.4	Valve ou section de valve
Essai en surcharge temporaire maximale	6.5	Valve ou section de valve
Essai sous tension continue minimale	6.6	Valve ou section de valve
Essai de support de valve sous tension continue	7.3.2	Support de valve
Essai de support de valve sous tension alternative	7.3.3	Support de valve
Essai de support de valve sous tension de choc de manœuvre	7.3.4	Support de valve
Essai de support de valve sous tension de choc de foudre	7.3.5	Support de valve
Essai de MVU sous tension continue à la terre	8.4.1	MVU
Essai de MVU sous tension alternative	8.4.2	MVU
Essai de MVU sous tension de choc de manœuvre	8.4.3	MVU
Essai de MVU sous tension de choc de foudre	8.4.4	MVU
Essai de valve sous tension alternative-continue	9.4.1 ou 9.4.2	Valve ou section de valve
Essai de valve sous tension de choc de manœuvre	9.4.3.2	
Essai de valve sous tension de choc de foudre	9.4.3.3	
Essai de blocage de l'IGBT en cas de surintensité	10	Valve ou section de valve
Essai de courant de court-circuit	11	Valve ou section de valve
Essai d'insensibilité de la valve aux perturbations électromagnétiques	12	Valve ou section de valve
NOTE Il convient que la section de valve utilisée dans l'essai de valve sous tension alternative-continue (9.4.1 ou 9.4.2), l'essai de valve sous tension de choc de manœuvre (9.4.3.2) et l'essai de valve sous tension de choc de foudre (9.4.3.3) soit une structure unique représentative de la conception diélectrique de la valve.		

6 Essais de fonctionnement

6.1 Objectif des essais

Les principaux objectifs des essais de fonctionnement sont de:

a) vérifier l'adéquation du niveau de la paire VSC/diode et des circuits électriques associés dans une valve en fonction des contraintes de courant, de tension et de température à l'état conducteur, lors de l'ouverture et de la fermeture dans les conditions de contraintes répétitives les plus défavorables;

b) démontrer l'interaction correcte entre l'électronique de la valve et les circuits de puissance des valves à VSC.

6.2 Objet d'essai

Les essais peuvent être réalisés soit sur une valve complète, soit sur des sections de valve. Le choix dépend principalement de la conception de la valve et des installations d'essai disponibles. Les essais spécifiés dans le présent article sont applicables aux sections de valve contenant cinq niveaux de valve ou plus, connectés en série. Si des essais utilisant moins de cinq niveaux sont proposés, des facteurs de sécurité d'essai supplémentaires doivent être convenus. En aucun cas, le nombre de niveaux connectés en série ne doit être inférieur à trois pour les essais.

La valve ou les sections de valve en essai doivent être assemblées avec tous les composants auxiliaires. Pour les valves équipées d'un parafoudre, un parafoudre de valve à échelle réduite peut être inclus.

Le fluide de refroidissement doit être dans un état représentatif des conditions de service. Le débit et la température, en particulier, doivent être établis en fonction des valeurs les plus défavorables correspondant à l'essai en question, de sorte que la ou les températures de composants appropriées soient égales aux valeurs applicables en service.

6.3 Circuit d'essai

Dans les conceptions dans lesquelles la valve agit comme une source de tension commandable et dispose d'une capacité à courant continu intégrée, la capacité à courant continu et ses connexions aux composants à semiconducteur font partie intégrante de l'objet d'essai.

Cependant, dans les conceptions dans lesquelles la valve fonctionne à la manière d'un commutateur et où le condensateur à courant continu est distinct de la valve, il est nécessaire que le condensateur à courant continu soit correctement représenté dans le circuit d'essai. En particulier, l'inductance de fuite en série des connexions entre le condensateur à courant continu et la valve, ainsi que la capacité parasite au niveau de la section de valve, doivent être correctement reproduites et mises à l'échelle en fonction de la taille de la section de valve en essai. Les interconnexions du circuit d'essai doivent être représentatives du type utilisé dans le convertisseur, afin de ne pas introduire de niveaux d'amortissement peu réalistes dus à des effets de peau.

6.4 Essai en service permanent maximal

Il est nécessaire que l'essai reproduise les paramètres suivants basés sur les conditions de service du convertisseur les plus défavorables. Plusieurs essais peuvent également être nécessaires pour reproduire tous les paramètres à leurs valeurs maximales.

Pour les valves à VSC:

- température maximale de jonction de l'IGBT en régime permanent;
- température maximale de jonction de la DRL en régime permanent;
- lorsque des circuits d'amortissement sont utilisés, température maximale des composants d'amortissement en régime permanent;
- tension et courant maximaux d'amorçage et de blocage en régime permanent.

Pour les valves à diode:

- température maximale de jonction de la diode en régime permanent;
- lorsque des circuits d'amortissement sont utilisés, température maximale des composants d'amortissement en régime permanent;
- tension et courant maximaux d'amorçage et de désamorçage de la diode en régime permanent.

Il est nécessaire que tous ces paramètres soient reproduits au cours de l'essai en service permanent maximal. Ils peuvent être reproduits dans le cadre d'essais séparés ou sous la forme d'un essai combiné.

La tension d'essai doit être basée sur la tension continue en régime permanent maximal, la fréquence de commutation d'essai doit être fondée sur la fréquence de commutation en régime permanent maximal et le modèle de modulation doit être représentatif de celui utilisé en service.

Le courant d'essai, en valeur efficace, doit être déterminé en tenant compte des harmoniques de courant et de tout autre courant supplémentaire circulant dans la valve.

La valeur du courant d'essai doit intégrer un facteur de sécurité d'essai de 1,05.

Pour une valve de type commutateur, la tension d'essai U_{tpv1} correspondant à la tension continue en régime permanent maximal doit être déterminée de la façon suivante:

$$U_{tpv1} = U_{dmax} \times k_n \times k_1$$

où

U_{dmax} est la tension continue en régime permanent maximal de la valve, y compris l'ondulation;

k_n est un facteur d'échelle d'essai selon 4.3.1;

k_1 est un facteur de sécurité d'essai;

k_1 = 1,05.

Pour une valve de type à source de tension commandable, la tension d'essai, U_{tpvl1}, par niveau de valve, doit être déterminée de la façon suivante:

$$U_{tpvl1} = U_{cmax} \times k_1$$

où

U_{cmax} est la tension continue en régime permanent maximal du niveau de valve, y compris l'ondulation;

k_1 est un facteur de sécurité d'essai;

k_1 = 1,05.

La durée de l'essai ne doit pas être inférieure à 30 min après la stabilisation de la température du fluide de refroidissement en sortie.

6.5 Essai en surcharge temporaire maximale

Si la valve est spécifiée pour un fonctionnement en surcharge temporaire, un essai en service temporaire maximal doit être réalisé.

NOTE La capacité des valves à convertisseur fonctionnant en surcharge temporaire maximale est généralement de quelques secondes, le refroidissement de la valve étant alors impossible.

Les conditions d'essai, lorsqu'elles sont exigées, doivent être déterminées en appliquant la même méthodologie qu'en 6.4 ci-dessus. Cependant, le courant d'essai doit être le courant de surcharge spécifié sans facteur de sécurité d'essai.

Avant l'essai, la valve ou la section de valve doit être amenée à un équilibre thermique dans les conditions indiquées en 6.4. L'essai en service temporaire maximal est alors engagé à partir de cette condition initiale et poursuivi pendant une durée égale à la durée de la surcharge temporaire multipliée par 1,2.

À l'issue du fonctionnement en surcharge temporaire, rétablir les conditions de régime permanent maximal spécifiées en 6.4 et les maintenir stables pendant 10 min.

6.6 Essai sous tension continue minimale

Le but de cet essai est de vérifier le bon fonctionnement des conceptions de valve dans lesquelles l'énergie des circuits électroniques de la valve provient de la tension apparaissant entre les bornes de la valve.

L'essai consiste à appliquer une tension continue entre les bornes de la valve ou section de valve. Pour cet essai, seule la tension est importante, le courant étant secondaire.

Le fonctionnement correct des circuits électroniques de la valve peut être démontré soit en débloquant la valve ou la section de valve, soit en prolongeant l'état bloqué et en surveillant les signaux de retour de données de l'électronique de la valve.

La tension d'essai U_{min} est définie de la façon suivante:

$$U_{\text{min}} = \frac{N_{\text{tut}}}{N_{\text{t}}} \times U_{\text{W}} \times k_2$$

où

U_{W} est la tension continue minimale d'une valve en service où le fonctionnement correct de l'électronique de la valve est exigé;

N_{tut} est le nombre de niveaux de VSC en essai, connectés en série;

N_{t} est le nombre total de niveaux de VSC connectés en série dans une valve unique, redondance incluse;

k_2 est un facteur de sécurité d'essai;

k_2 = 0,95.

La durée de l'essai ne doit pas être inférieure à 10 min.

7 Essais diélectriques sur la structure de support de valve

7.1 Objectif des essais

Les principaux objectifs de ces essais sont de:

a) vérifier la capacité de tenue en tension au niveau de l'isolation du support de valve, des conduits de refroidissement, des conduits de lumière et d'autres composants isolants associés au support de valve. S'il existe une isolation à la terre autre que le support de valve, des essais supplémentaires peuvent alors être nécessaires;

b) vérifier que les tensions d'allumage et d'extinction des décharges partielles sont supérieures à la tension de fonctionnement maximale présente sur le support de valve.

NOTE Selon l'application, il est possible d'éliminer certains des essais réalisés sur le support de valve, après accord entre l'acheteur et le fournisseur.

7.2 Objet d'essai

Le support de valve à utiliser pour les essais peut être un objet représentatif distinct comprenant une représentation des parties adjacentes de la valve, ou il peut faire partie de l'assemblage utilisé pour les essais de valve unique ou d'ensemble à valves multiples. Il doit être assemblé avec tous les composants auxiliaires en place et les surfaces au potentiel de terre adjacentes doivent être correctement représentées. La proximité des surfaces au potentiel de terre adjacentes (matériel ou infrastructure de bâtiment) doit être évaluée et la représentation incluse le cas échéant. Pour les distances d'isolement nettement supérieures à celles déterminées par les exigences relatives à la coordination de l'isolement, par exemple des distances d'isolement imposées à la place des exigences d'accès, il peut alors être envisagé d'omettre les surfaces au potentiel de terre à ces emplacements. Si une valve unique est composée d'une seule structure, sa grande taille peut parfois rendre impossible l'essai de la valve complète dans un laboratoire. Dans ces cas, il est admis d'effectuer les essais de structure de support de valve sur une section préassignée de la structure de support, à condition de pouvoir démontrer que la conception de l'objet d'essai est représentative de la conception de la structure complète et que les essais couvrent les contraintes les plus défavorables exercées sur toute partie de la structure de support de la valve.

Pour les besoins de l'essai, le fluide de refroidissement doit être dans un état représentatif des conditions de service les plus pénalisantes.

Si une valve unique est composée de plusieurs structures de sorte qu'il existe plusieurs structures de support de valve par valve, il doit alors être démontré que les essais proposés couvrent les contraintes les plus défavorables exercées sur toute structure de support de valve.

7.3 Exigences d'essai

7.3.1 Généralités

Tous les niveaux d'essai indiqués ci-dessous sont soumis à une correction atmosphérique selon la description donnée en 4.2.

7.3.2 Essai de support de valve sous tension continue

Les deux bornes principales de la valve doivent être connectées entre elles, puis la tension continue doit être appliquée entre les deux bornes principales ainsi connectées et la terre. À partir d'une tension égale au maximum à 50 % de la tension d'essai pendant 1 min, la tension doit être élevée le plus rapidement possible à la tension d'essai spécifiée à maintenir pendant 1 min, être maintenue constante pendant 1 min, réduite à la tension d'essai spécifiée à maintenir pendant 3 h, maintenue constante pendant 3 h, puis réduite à zéro. Durant la dernière heure de l'essai de 3 h spécifié, le nombre de décharges partielles dépassant 300 pC doit être enregistré comme décrit à l'Annexe B de l'IEC 60700-1:2015+AMD1:2021.

Le nombre d'impulsions supérieures à 300 pC ne doit pas dépasser 15 impulsions par minute, selon une moyenne établie sur l'ensemble de la période d'enregistrement. Parmi celles-ci, pas plus de sept impulsions par minute ne doivent dépasser 500 pC, pas plus de trois impulsions par minute ne doivent dépasser 1 000 pC, et pas plus d'une impulsion par minute ne doit dépasser 2 000 pC.

Si une tendance croissante est observée au niveau de l'amplitude ou du taux de décharge partielle, la durée de l'essai peut être prolongée après accord mutuel entre l'acheteur et le fournisseur.

L'essai doit alors être répété avec une tension de polarité opposée.

Préalablement à l'essai et avant de répéter l'essai avec une tension de polarité opposée, le support de valve peut être court-circuité et mis à la terre pendant plusieurs heures. Cette procédure peut être répétée à la fin de l'essai sous tension continue.

La tension d'essai continue du support de valve U_{tds} doit être déterminée de la façon suivante:

essai de 1 min

$$U_{tds} = \pm U_{dmS1} \times k_3 \times k_t$$

essai de 3 h

$$U_{tds} = \pm U_{dmS2} \times k_3$$

où

U_{dmS1} est la tension maximale de courte durée apparaissant au niveau du support de valve, telle que déterminée par des études de coordination de l'isolement. U_{dmS1} doit être la valeur la plus élevée entre (a) la tension moyenne maximale sur une période de 1 s et (b) la tension moyenne entre l'instant où la tension de crête apparaît et l'instant où la tension diminue rapidement par l'action de dispositifs à décharge rapide ou de la reconfiguration, le cas échéant;

U_{dmS2} est la valeur maximale de la composante continue de la tension de fonctionnement en régime permanent apparaissant au niveau du support de valve;

k_3 est un facteur de sécurité d'essai;

k_3 = 1,10 pour l'essai de 1 min;

k_3 = 1,15 pour l'essai de 3 h;

k_t est le facteur de correction atmosphérique selon 4.2.

7.3.3 Essai de support de valve sous tension alternative

Pour effectuer l'essai, les deux bornes principales de la valve doivent être connectées entre elles, puis la tension alternative doit être appliquée entre les deux bornes principales ainsi connectées et la terre.

À partir d'une tension égale au maximum à 50 % de la tension d'essai pendant 1 min, la tension doit être élevée à la tension d'essai spécifiée à maintenir pendant 1 min, être maintenue constante pendant 1 min, réduite à la tension d'essai spécifiée à maintenir pendant 30 min, maintenue constante pendant 30 min, puis réduite à zéro.

Avant la fin de l'essai de 30 min, le niveau de décharge partielle doit être surveillé et enregistré sur une période de 1 min. Si la valeur de décharge partielle est inférieure à 200 pC, la structure peut être acceptée sans condition. Si la valeur de décharge partielle est supérieure à 200 pC, les résultats d'essai doivent être évalués.

La tension d'essai alternative du support de valve U_{tas} doit être déterminée de la façon suivante:

essai de 1 min:

$$U_{tas} = \frac{U_{mS1}}{\sqrt{2}} \times k_4 \times k_t$$

essai de 30 min

$$U_{\text{tas}} = \frac{U_{\text{mS2}}}{\sqrt{2}} \times k_4$$

où

U_{mS1} est la valeur de crête de la tension maximale présente sur le support de valve en service, en particulier en condition de défaut du système et en condition de fonctionnement en défaut de la valve. L'effet limitatif en surtension du parafoudre de phase ou d'autres dispositifs de protection contre les surtensions, le cas échéant, doit être pris en compte pour en déduire cette surtension;

U_{mS2} est la valeur de crête de la tension de fonctionnement répétitive maximale au niveau du support de valve pendant le fonctionnement en régime permanent, y compris le dépassement de commutation;

k_4 est un facteur de sécurité d'essai;

k_4 = 1,10 pour l'essai de 1 min;

k_4 = 1,15 pour l'essai de 30 min;

k_t est le facteur de correction atmosphérique selon 4.2.

7.3.4 Essai de support de valve sous tension de choc de manœuvre

L'essai doit comprendre trois applications de tensions de choc de manœuvre de polarité positive et trois applications de tensions de choc de manœuvre de polarité négative entre les bornes principales de la valve (connectées entre elles) et la terre.

Une forme d'onde de tension de choc de manœuvre normalisée, conforme à l'IEC 60060, doit être utilisée.

La tension d'essai doit être choisie conformément à la coordination de l'isolement du poste VSC.

7.3.5 Essai de support de valve sous tension de choc de foudre

L'essai doit comprendre trois applications de tensions de choc de foudre de polarité positive et trois applications de tensions de choc de foudre de polarité négative entre les bornes principales de la valve (connectées entre elles) et la terre.

Une forme d'onde de tension de choc de foudre normalisée, conforme à l'IEC 60060, doit être utilisée.

La tension d'essai doit être choisie conformément à la coordination de l'isolement du poste VSC.

8 Essais diélectriques sur un ensemble à valves multiples

8.1 Généralités

Le présent article s'applique uniquement si au moins deux valves sont installées dans une structure de valve commune (ensemble à valves multiples). Si chaque valve est montée individuellement dans sa propre structure de valve, le présent article ne s'applique pas.

8.2 Objectif des essais

Les principaux objectifs de ces essais sont de:

a) vérifier la capacité de tenue en tension de l'isolation externe du MVU, par rapport à son environnement, en particulier pour la ou les valves connectées au potentiel du pôle;

b) vérifier la capacité de tenue en tension entre des valves uniques dans une structure de MVU;

c) vérifier que les niveaux de décharge partielle se situent dans les limites spécifiées.

8.3 Objet d'essai

De nombreuses dispositions de valves et d'ensembles à valves multiples sont possibles. L'objet ou les objets d'essai doivent être choisis afin de refléter, aussi précisément que possible, la configuration en service des valves, dans la mesure où cela est nécessaire pour l'essai en question. L'objet d'essai doit être entièrement équipé à moins qu'il soit possible de démontrer que la simulation ou l'omission de certains composants ne rend pas les résultats moins significatifs.

Des valves individuelles peuvent devoir être court-circuitées en fonction de la configuration du MVU et des objectifs de l'essai.

Lorsque la borne à basse tension du MVU n'est pas connectée au potentiel de terre, des précautions doivent être prises afin d'effectuer une terminaison convenable de la borne à basse tension du MVU au cours des essais pour simuler correctement la tension existant au niveau de cette borne. Des plans de masse, dont la séparation doit être déterminée en fonction de la proximité d'autres valves et des surfaces au potentiel de terre, doivent être utilisés.

8.4 Exigences d'essai

8.4.1 Essai de MVU sous tension continue à la terre

La tension d'essai continue doit être appliquée entre la borne à courant continu de potentiel le plus élevé du MVU et la terre.

À partir d'une tension égale au maximum à 50 % de la tension d'essai pendant 1 min, la tension doit être élevée le plus rapidement possible à la tension d'essai spécifiée à maintenir pendant 1 min, être maintenue constante pendant 1 min, réduite à la tension d'essai spécifiée à maintenir pendant 3 h, maintenue constante pendant 3 h, puis réduite à zéro.

Dans la mesure du possible, la tension d'essai doit être augmentée de 50 % jusqu'au niveau de tension de l'essai pendant 1 min en moins de 10 s environ.

Pendant la dernière heure de l'essai de 3 h spécifié, le nombre de décharges partielles dépassant 300 pC doit être enregistré.

Le nombre d'impulsions supérieures à 300 pC ne doit pas dépasser 15 impulsions par minute, selon une moyenne établie sur l'ensemble de la période d'enregistrement. Parmi celles-ci, pas plus de sept impulsions par minute ne doivent dépasser 500 pC, pas plus de trois impulsions par minute ne doivent dépasser 1 000 pC, et pas plus d'une impulsion par minute ne doit dépasser 2 000 pC.

Si une tendance croissante est observée au niveau de l'amplitude ou du taux de décharge partielle, la durée de l'essai peut être prolongée après accord mutuel entre l'acheteur et le fournisseur.

L'essai doit alors être répété avec une tension de polarité opposée.

Préalablement à l'essai et avant de répéter l'essai avec une tension de polarité opposée, les bornes du MVU peuvent être court-circuitées ensemble et mises à la terre pendant plusieurs heures. Cette procédure peut être répétée à la fin de l'essai sous tension continue.

La tension d'essai continue du MVU U_{tdm} doit être déterminée de la façon suivante:

essai de 1 min

$$U_{\text{tdm}} = \pm U_{\text{dmm1}} \cdot k_5 \cdot k_t$$

essai de 3 h

$$U_{\text{tdm}} = \pm U_{\text{dmm2}} \times k_5$$

où

U_{dmm1} est la tension maximale de courte durée apparaissant entre la borne à haute tension du MVU et la terre, telle que déterminée par des études de coordination de l'isolement; U_{dmm1} doit être la valeur la plus élevée entre (a) la tension moyenne maximale sur une période de 1 seconde et (b) la tension moyenne entre l'instant où la tension de crête apparaît et l'instant où la tension diminue rapidement par l'action de dispositifs à décharge rapide ou de la reconfiguration, le cas échéant;

U_{dmm2} est la valeur maximale de la composante de courant continu de la tension de fonctionnement en régime permanent apparaissant entre la borne à haute tension du MVU et la terre;

k_5 est un facteur de sécurité d'essai;

k_5 = 1,10 pour l'essai de 1 min;

k_5 = 1,15 pour l'essai de 3 h;

k_t est le facteur de correction atmosphérique selon 4.2.

8.4.2 Essai de MVU sous tension alternative

Si un MVU subit des contraintes de tension alternative ou composite alternative et continue entre deux bornes quelconques, dont la capacité de tenue n'est pas démontrée de façon adéquate par d'autres essais, il est alors nécessaire de réaliser un essai sous tension alternative entre les bornes concernées du MVU.

Pour réaliser l'essai, la source de tension d'essai doit être connectée à la paire de bornes du MVU en question. Le point de connexion à la terre dépend de la disposition du circuit d'essai.

À partir d'une tension égale au maximum à 50 % de la tension d'essai pendant 1 min, la tension doit être élevée à la tension d'essai spécifiée à maintenir pendant 1 min, être maintenue constante pendant 1 min, réduite à la valeur à maintenir pendant 30 min, maintenue constante pendant 30 min, puis réduite à zéro.

Avant la fin de l'essai de 30 min, le niveau de décharge partielle doit être surveillé et enregistré sur une période de 1 min. Si la valeur de décharge partielle est inférieure à 200 pC, la structure peut être acceptée sans condition. Si la valeur de décharge partielle est supérieure à 200 pC, les résultats d'essai doivent être évalués.