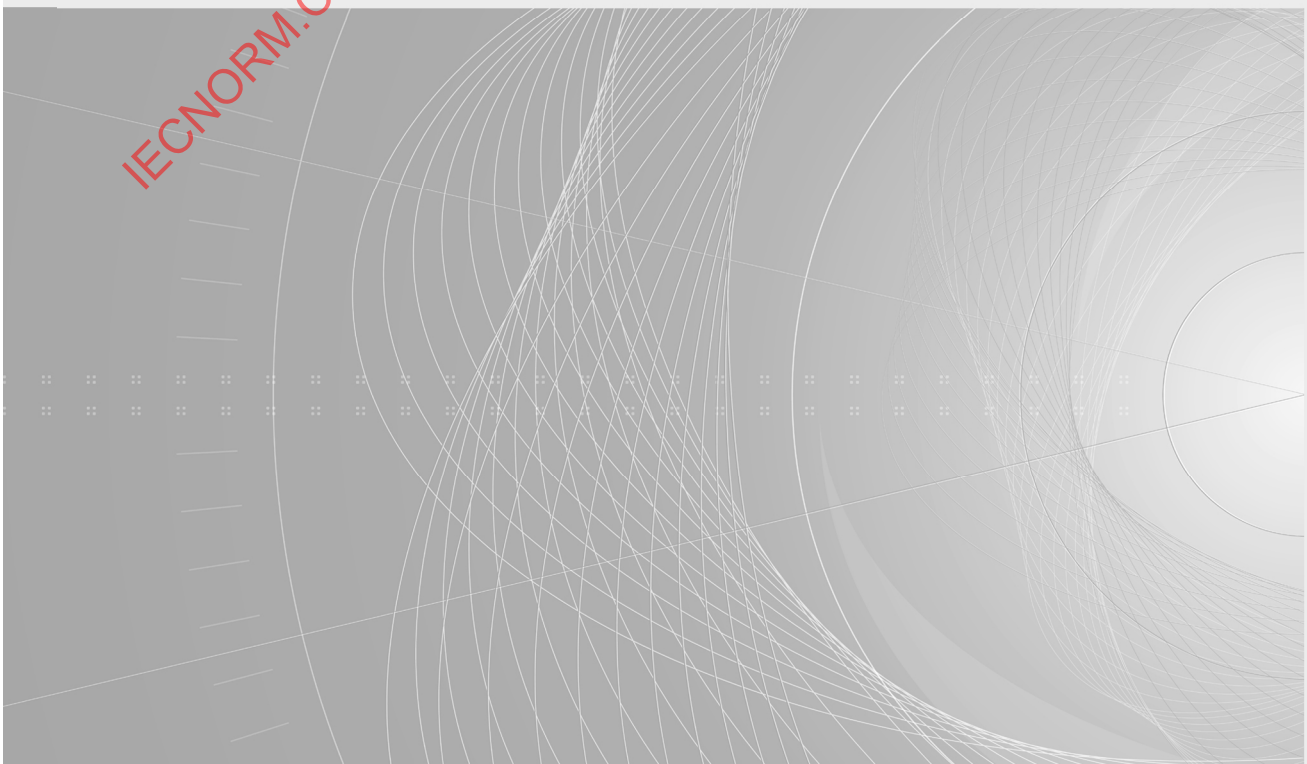
IEC 60747-15

Edition 3.0 2024-10
REDLINE VERSION

INTERNATIONAL STANDARD

colour inside

Semiconductor devices – ~~Discrete devices~~
Part 15: Discrete devices – Isolated power semiconductor devices



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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.080.99

ISBN 978-2-8322-9946-3

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – ~~DISCRETE DEVICES –~~

Part 15: Discrete devices – Isolated power semiconductor devices

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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This redline version of the official IEC Standard allows the user to identify the changes made to the previous edition IEC 60747-15:2010. A vertical bar appears in the margin wherever a change has been made. Additions are in green text, deletions are in strikethrough red text.

IEC 60747-15 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

This third edition cancels and replaces the second edition published in 2010. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) The intelligent power semiconductor modules (IPM), which was previously excluded from the first and second edition, is now included in this document (Annex C);
b) The thermal resistance is described for each switch (6.2.4);
c) Added isolation test between temperature sensor and terminals, in case there is an agreement with the user (6.1.2).

The text of this International Standard is based on the following documents:

Draft	Report on voting
47E/832/FDIS	47E/844/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

This International Standard is to be used in conjunction with IEC 60747-1:2006 and Amendment 1: 2010.

A list of all parts in the IEC 60747 series, published under the general title *Semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

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SEMICONDUCTOR DEVICES – ~~DISCRETE DEVICES –~~

Part 15: Discrete devices – Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the requirements for isolated power semiconductor devices ~~excluding devices with incorporated control circuits~~. These requirements are additional to those given in other parts of IEC 60747 for the corresponding non-isolated power devices and parts of IEC 60748 for ICs.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-1:2007, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60270:2015, *High-voltage test techniques – Partial discharge measurements*

IEC 60664-1:~~2007~~2020, *Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests*

IEC 60721-3-3:~~1994~~2019, *Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*
IEC 60747-1:2006/AMD1:2010

IEC 60747-2:2016, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6:2016, *Semiconductor devices – Part 6: Thyristors*

IEC 60747-7:2019, *Semiconductor discrete devices and integrated circuits – Part 7: Bipolar transistors*

IEC 60747-8:2021, *Semiconductor devices – Part 8: Field-effect transistors*

IEC 60747-9:2019, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 60748 (all parts), *Semiconductor devices – Integrated circuits*

IEC 60749-5:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-10:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock*

IEC 60749-12:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency*

IEC 60749-15:2020, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices*

IEC 60749-21:2011, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-25:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-34:2010, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
isolated power semiconductor device
semiconductor power device that contains an integral electrical insulator between the cooling surface or base plate and any isolated circuit elements

3.2
constituent parts of the isolated power semiconductor device

3.2.1
switch
any single component that performs a switching function in an electrical circuit, e.g. diode, thyristor, MOSFET, etc.

Note 1 to entry: A switch might be a parallel or series connection of several chips with a single functionality.

3.2.2
base plate
part of the package having a cooling surface that transfers the heat from inside to outside

3.2.3
main terminal
terminal having a high potential of the power circuit and carrying the main current

Note 1 to entry: The main terminal can comprise more than one physical connector.

3.2.4
control terminal
terminal having a low current capability for the purpose of control function, to which the external control signals are applied or from which sensing parameters are taken

3.2.4.1
high voltage control terminal
terminal electrically connected to an isolated circuit element, but carrying only low current for control function

Note 1 to entry: Examples include current shunts and collector sense terminals having the high potential of the main terminals.

3.2.4.2
low voltage control terminal
terminal having a control function and isolated from the high voltage control terminals

Note 1 to entry: Examples include the terminals of isolated temperature sensors and isolated gate driver inputs, etc.

3.2.5
insulation layer
integrated part of the device case that insulates any part having high potential from the cooling surface or external heat sink and any isolated circuit element

3.3
peak case non-rupture current
peak current, which will not lead to a rupture of the package, ejecting plasma and massive particles under specified conditions

3.4
thermal interface material
heat conducting material between base plate and external heat sink

4 Letter symbols

4.1 General

General letter symbols are defined in Clause 4 of IEC 60747-1:2006.

4.2 Additional subscripts/symbols

p parasitic

t terminal

isol isolation

~~m = mount~~

4.3 List of letter symbols

4.3.1 Voltages and currents

Terminal current	I_{tRMS}
Isolation voltage	V_{isol}
Partial discharge inception voltage	V_i
Partial discharge extinction voltage	V_e
Isolation leakage current	I_{isol}

~~Peak case non-rupture current (for diode and thyristor devices) I_{RSMC}~~

~~Peak case non-rupture current (for IGBT and MOSFET devices) I_{CNR}~~

4.3.2 Mechanical symbols

Mounting torque for screws to heat sink	M_s
Mounting torque for terminal screws	M_t
Mounting force	F
~~Maximum~~ Acceleration in all 3 axis (x, y, z)	a
Mass	m
Flatness of the case (base plate)	e_c
Flatness of the ~~cooling~~ heat sink surface ~~(heat sink)~~	e_s
Roughness of the case (base plate)	R_{Zc}
Roughness of the ~~cooling~~ heat sink surface ~~(heat sink)~~	R_{Zs}
Thickness of thermal interface material (case – heat sink)	$d_{(c\text{-}s)}$

4.3.3 Other symbols

~~Total maximum power dissipation per switch at T_c = 25 °C~~	~~P_{tot}~~
Parasitic inductance, effective between terminals and chips ~~(to be specified)~~	L_p
Parasitic capacitance between terminals and cooling surface (case, base plate, ground)	C_p
Lead resistance between terminal x and ~~related switch~~ internal device connection x'	r_{xx}
Terminal temperature	T_t
Number of power load cycles until failure of a percentage p of a population of devices	$N_{f;p}$

5 Essential ratings (limiting values) and characteristics

5.1 General

Isolated power semiconductor devices should be specified as case rated or heat sink rated devices. The ratings and characteristics should be quoted at a temperature of 25 °C or another specified elevated temperature. Requirements for multiple devices having a common encapsulation are described in 5.12 of IEC 60747-1:2006.

5.2 Ratings (limiting values)

5.2.1 Isolation voltage or isolation test voltage (V_{isol})

Maximum RMS or DC value between main terminals and high voltage control terminals at one side and low voltage control terminals (where appropriate) and base plate at the other side for a specified time.

5.2.2 Peak case non-rupture current ~~(I_{RSMC} or I_{CNR})~~ (where appropriate)

Maximum value for each main terminal that does not cause the bursting of the case or emission of plasma and particles.

5.2.3 Terminal current (I_{tRMS}) (where appropriate)

Maximum RMS value of the current through the main terminal under specified conditions at minimum mounting torque M_t and maximum allowed terminal temperature (T_{tmax} = T_{stg} or T_{tmax} ≤ T_{vjmax}).

~~#### 5.2.4 Total power dissipation (P_{tot})~~

~~Maximum value per switch at T_c = 25 °C (or T_s = 25 °C), when T_{vj} = T_{vjmax}, at d.c. load.~~

5.2.4 Temperatures

5.2.4.1 Solder temperature (T_{sold}) (where appropriate)

Maximum solder temperature T_{sold} during solder process over a specified solder processing time t_{sold}.

5.2.4.2 Storage temperature (T_{stg})

Minimum and maximum storage temperature.

5.2.5 Mechanical ratings

5.2.5.1 Mounting torque for screws to heat sink (M_s)

Minimum and maximum mounting torque that shall be applied to the fixing screws to the heat sink.

5.2.5.2 Mounting torque for screws to terminals (M_t)

Minimum and maximum mounting torque that shall be applied to screwed terminals.

5.2.5.3 Mounting force (F)

Minimum and maximum mounting force for pressure mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device.

5.2.5.4 Terminal pull-out force (F_t)

Maximum force.

5.2.5.5 Acceleration (a)

Maximum value along each axis (x, y, z).

5.2.5.6 Flatness of the heat sink surface (e_s) (where appropriate)

Maximum deviation from flatness for the heat sink surface over the whole mounting area.

5.2.5.7 Roughness of the heat sink surface (R_{Zs}) (where appropriate)

Maximum roughness of the heat sink surface over the whole mounting area.

5.2.6 Climatic ratings (where appropriate)

Limiting values of environmental parameters for the final application as follows:

– ambient temperature;
– humidity;
– speed and pressure of air;
– irradiation by sun and other heat sources;
– mechanical active substances;
– chemically active substances;
– biological issues,

shall be described in classes as specified in IEC 60721-3-3:~~1994~~2019, Table 1.

5.3 Characteristics

5.3.1 Mechanical characteristics

5.3.1.1 Creepage distance along surface (d_s)

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate.

NOTE 1 IEC 60112:2020 (details to comparative tracking index "CTI") and IEC 60664-1:~~2007~~2020, 5.2 apply.

NOTE 2 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance considerably (details see 60664-1:~~2007~~2020, examples). This is essential, if dust, moisture or dirt starts to cover the surface and increases the leakage current over surface, which might start burning the plastic encapsulation material.

5.3.1.2 Clearance distance in air (d_a)

Minimum value of distance through air between terminals of different potential of the isolated device and to base plate.

NOTE For details, see IEC 60664-1:~~2007~~2020, 4.6 and 5.1 which show typical examples of various shapes of clearance distances.

5.3.1.3 Mass (m) of the device

Maximum value excluding accessories (mounting hardware).

5.3.1.4 Flatness of the case (base plate) (e_c) (where appropriate)

Maximum and minimum allowed deviation from flatness for the base plate and its direction (convex or concave).

5.3.2 Parasitic inductance (L_p)

Maximum or typical value between the main terminals of each main current path.

5.3.3 Parasitic capacitances (C_p)

Maximum value of parasitic capacitance between the specified main terminal(s) and the cooling surface.

5.3.4 Partial discharge inception voltage (V_{iM} or $V_{i(RMS)}$) (where appropriate)

Minimum peak value V_{iM} or RMS value $V_{i(RMS)}$ between the isolated terminals and the base plate (details, see IEC 60270:2015).

5.3.5 Partial discharge extinction voltage (V_{eM} or $V_{e(RMS)}$) (where appropriate)

Minimum peak value V_{eM} or RMS value $V_{e(RMS)}$ between the isolated terminals and the base plate (for details, see IEC 60270:2015).

5.3.6 Thermal resistances

5.3.6.1 Thermal resistance junction to case for case rated devices ($R_{th(j-c)X}$)

Maximum value of thermal resistance junction to a specified reference point at the case (base plate) per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)).

5.3.6.2 Thermal resistance case to heat sink ($R_{th(c-s)}$) (where appropriate)

Maximum or typical value of thermal resistance between two specified points at the case and at the heat sink of the case rated device ("module"), when the case is mounted according to manufacturer's mounting instructions.

5.3.6.3 Thermal resistance case to heat sink per switch ($R_{th(c-s)X}$) (where appropriate)

Maximum or typical value of thermal resistance between the two specified points of the case and the heat sink of the switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)) of the isolated case rated devices ("module"), when the case is mounted according to the manufacturer's mounting instructions.

5.3.6.4 Thermal resistance junction to heat sink for heat sink rated devices ($R_{th(j-s)X}$)

Maximum or typical value of thermal resistance junction to a specified point at the heat sink per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)), when the device is mounted according to the manufacturer's mounting instructions.

5.3.6.5 Thermal resistance junction to sensor ($R_{th(j-r)}$) (where appropriate)

Value of thermal resistance junction to an integrated temperature sensor when the device is mounted according to the manufacturer's mounting instructions.

~~NOTE~~ The position of this thermal resistance should be shown in the thermal resistance equivalent circuit.

5.3.7 Transient thermal impedance (Z_{th})

Thermal impedance as a function of the time elapsed after a step change of power dissipation for each thermal resistance specified in 5.3.6 and shall be specified in one of the following ways.

6 Measurement methods

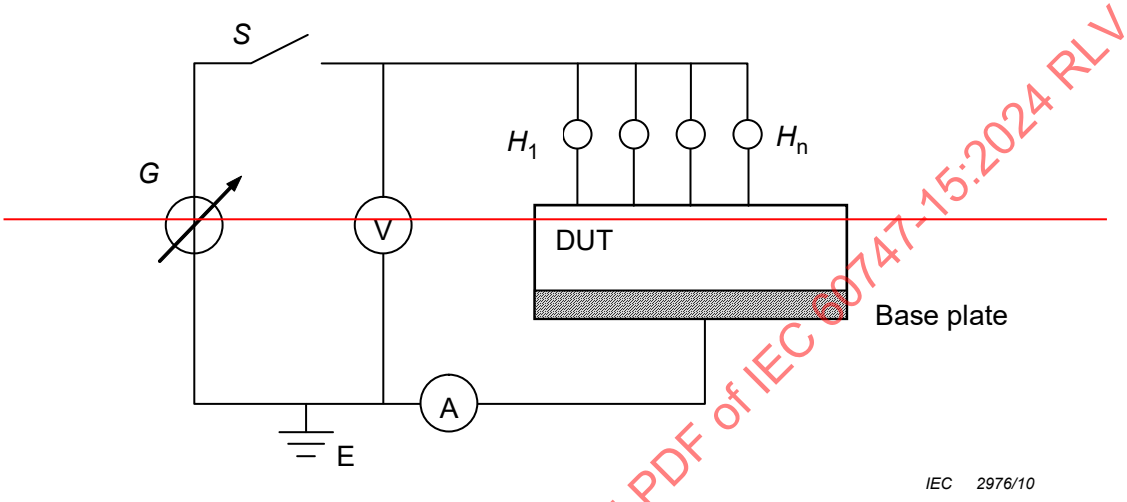
6.1 Verification of isolation voltage rating

6.1.1 Verification of isolation voltage rating between terminals and base plate (V_{isol})

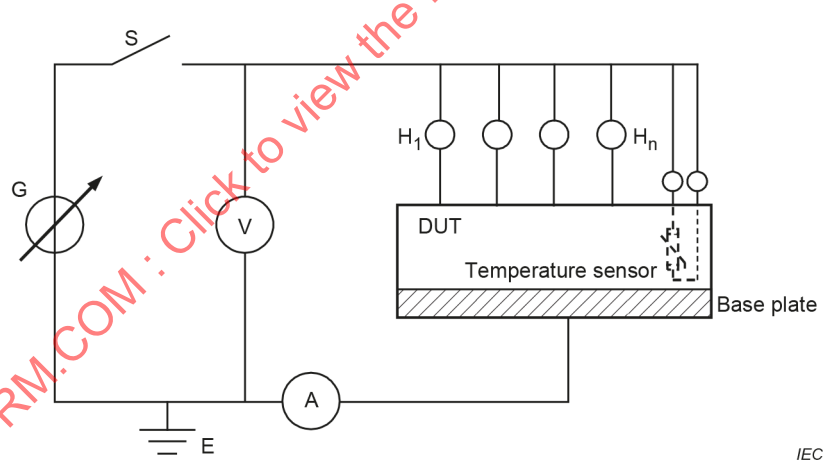
– Purpose

Proof of the ability of the isolated power device to withstand the rated isolation voltage.

– Circuit diagram



See Figure 1.



Key

DUT	device under test
G	voltage source with high impedance, capable to supply V_{isol}
S	main switch
V	voltmeter for V_{isol}
A	ammeter or current probe for Iisol
H_1...H_n	high potential terminal

Figure 1 – Basic circuit diagram for isolation breakdown withstand voltage test ("high pot test") with V_{isol}

The voltage source G is capable to supply the isolation voltage V_{isol} as the AC or DC voltage with a high internal impedance to limit the possible breakthrough current in case of breakdown of the DUT.

All main terminals and high voltage control terminals are connected together and connected to the high potential output terminal H of the voltage source G. The base plate of the DUT, respectively its metallized cooling surface and all low voltage terminals are connected to ground potential E. An amperemeter or current probe A is applied to measure the isolation leakage current.

If there is an agreement with user, perform an isolation test between the temperature sensor and the terminals (V_{Isol1}) (See 6.1.2).

– Test procedure

Switch S is closed and the voltage is slowly raised to the specified value and maintained at that value for the specified time. The current measured on ammeter A shall not exceed the specified value. The voltage is then reduced to zero.

– Specified conditions

Specified in IEC 60664-1:~~2007~~2020.

- Ambient or case temperature
- V_{isol}
- I_{isol} as maximum test limit
- Test time t, if less than 60 s.

6.1.2 Verification of isolation voltage rating between temperature sensor and terminals (V_{isol1})

– Purpose

To verify that the isolation voltage between the temperature sensor and the other terminals in case the temperature sensor is connected to the base plate potential.

– Circuit diagram

See Figure 2.

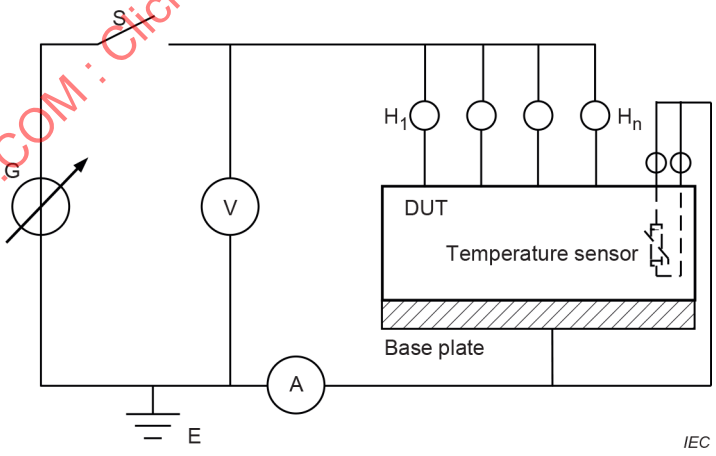


Figure 2 – Basic circuit diagram for isolation voltage test between temperature sensor and terminals (V_{isol1})

– Circuit description and requirements, test procedure and specified conditions

Similar as described in 6.1.1, but optionally a lower test voltage V_{isol1} may be specified and applied.

6.2 Methods of measurement

6.2.1 Partial discharge inception and extinction voltages (V_i) (V_e)

Between high potential terminals and base plate (where appropriate). See IEC 60270:2015 and IEC 60664-1:~~2007~~2020.

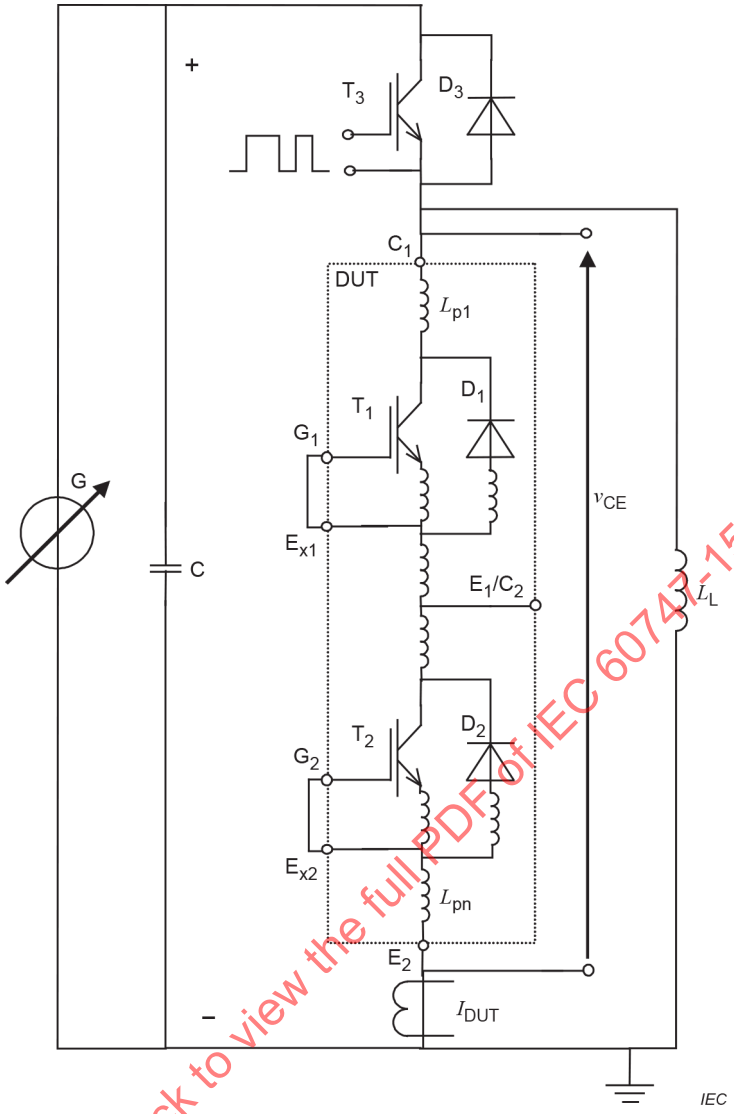
6.2.2 Parasitic inductance (L_p)

– Purpose

To measure the parasitic inductance between two main terminals.

– Circuit diagram

See Figure 3.



Key

DUT	device under test T_1+T_2, for example IGBT (Single or Dual – shown – or branch of a three phase arrangement), fast diode or MOSFET device
C	main capacitor bank as reservoir
L_L	load inductance, at least 100 times the parasitic inductance
L_{p1} ...L_{pn}	portions of parasitic inductance L_p
I_{DUT}	current probe
G	voltage source to charge the capacitor
T_1	DUT, top switch (shown as IGBT in Figure 3)
T_2	DUT, bottom switch (shown as IGBT in Figure 3), optional
T_3	auxiliary IGBT switch

Figure 3 – Circuit diagram for measurement of parasitic inductances (L_p)

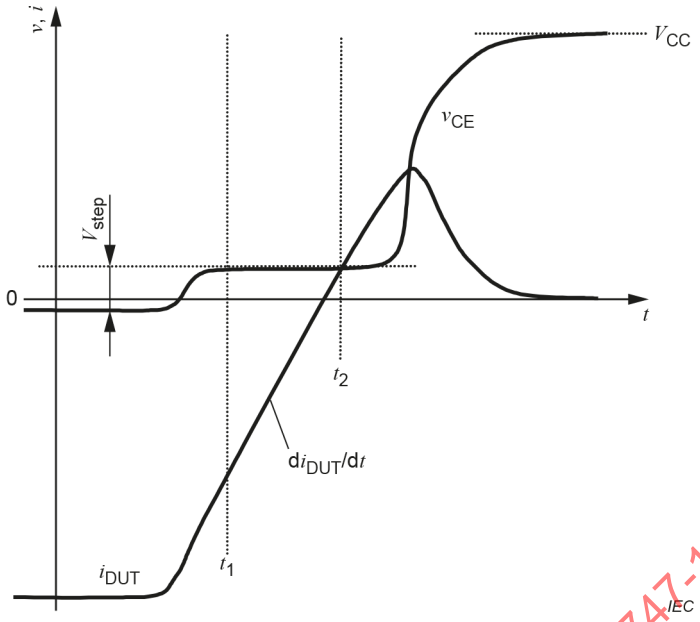


Figure 4 – Wave forms

– Circuit description and requirements

The circuit of Figure 3 consists of a DC supply G for the charge reservoir C; T_3 is an auxiliary switch, a gate drive unit for T_3, the DUT inserted into the test set-up with the gate control terminals shorted, a dual channel oscilloscope, which senses the voltage v_{CE} between main terminals "C_1" and "E_2", a current probe, which senses the current i_{DUT} through the diode path of the DUT, connected to the dual channel oscilloscope. This measuring method uses reduced voltage V_{CC} and the di/dt of diodes incorporated in the device at switch-off, sensing the voltage at outside main terminals. This is usable for single switch devices as well as for half bridge circuit devices (DUAL modules).

– Measurement procedure

The waveforms observed by this measurement shown in Figure 4.

A pulsed current method is used. Auxiliary transistor T_3 switches the load current to the inductor L_L on and off. When T_3 is off, the current freewheels via the diodes of the DUT. When T_3 switches on again, it causes the current through the diodes to fall at an almost linear rate di_{DUT}/dt. During this time (t_1 –t_2), the voltage across the DUT forms at step of V_{step} caused by the internal parasitic inductance at current decline (di_{DUT}/dt). The value of the parasitic inductance of the main current path can be calculated from

$$L_p = V_{step} / |(di_{DUT}/dt)| \quad (1)$$

NOTE Use low inductance (sheeted) bus baring and low inductance current probe.

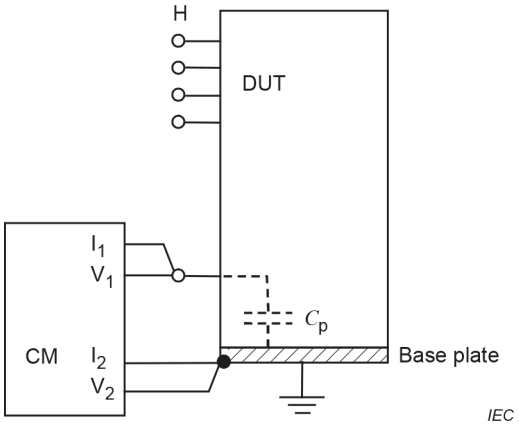
6.2.3 Parasitic capacitance terminal to case (C_p)

– Purpose

To measure the parasitic capacitance C_p between specified main terminal(s) and the case (base plate)

– Circuit diagram

See Figure 5.



Key

C_p parasitic capacitance

H high potential terminal

CM capacitance meter

Figure 5 – Circuit diagram for measurement of parasitic capacitance (C_p)

– Measurement procedure

Mount the device to a grounded heat sink according to the manufacturer's mounting instructions. Connect the current source connector "I_1" of the capacitance meter CM to the specified terminal and connector "I_2" to ground (base plate) of the DUT. Connect the voltage sensing connector of the capacitance meter to test points "V_1" and "V_2" to ground. CM is set to the specified frequency. The capacitance C_p can be read on CM. For the measurement of the total coupling capacitance C_p connect all main terminals to each other and proceed with the measurement as described above.

– Specified conditions

- Measurement frequency f of the CM.

6.2.4 Thermal characteristics

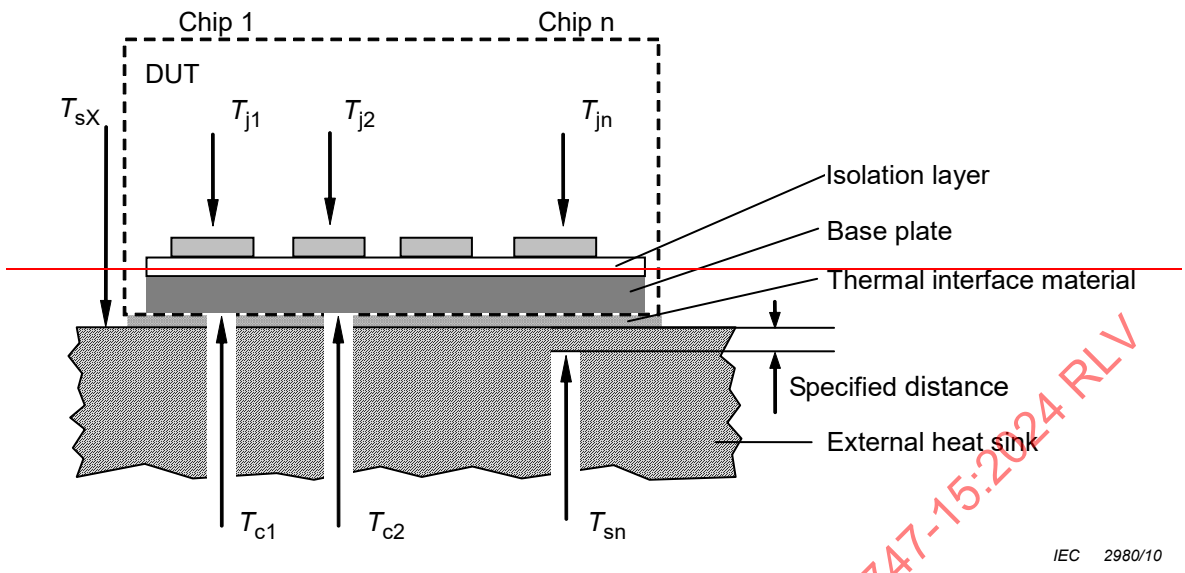
6.2.4.1 General description of measuring methods

– Purpose

To measure thermal characteristics between the switch and the cooling system.

– Reference points for temperature measurement and description

Same methods should be used as for the corresponding non-isolated device. Thermal resistance and impedance are measured in the same way as described in the documents for diodes IEC 60747-2:2016, thyristors IEC 60747-6:2016, bipolar transistors IEC 60747-7:2019, FETs IEC 60747-8:2021 and IGBTs IEC 60747-9:2019.



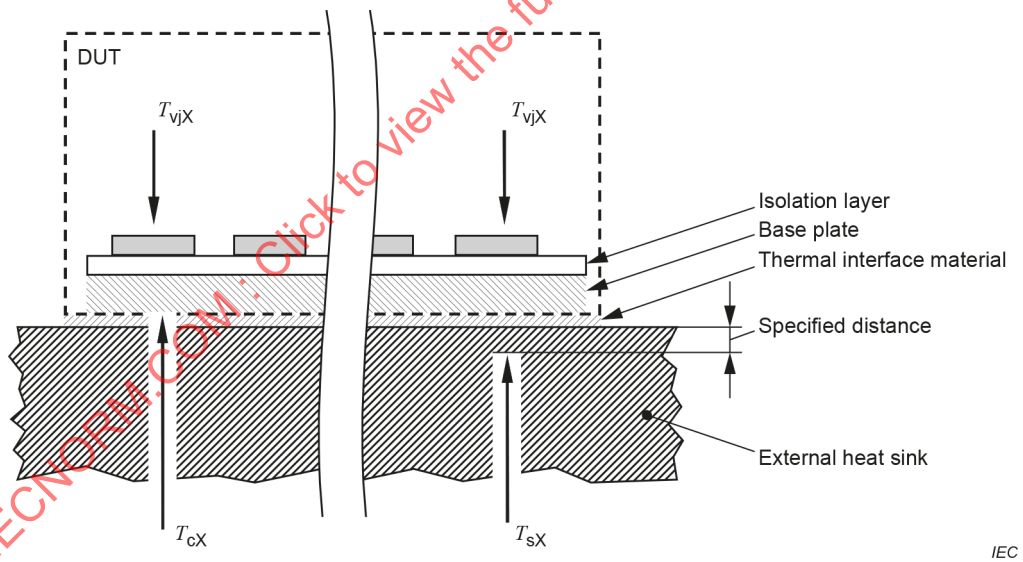
~~**Key**~~

~~$T_{j1...n}$ – junction temperature of chip 1 to n~~

~~$T_{c1...n}$ – case temperature under chip 1 to n~~

~~$T_{s1...n}$ – heatsink temperature under chip 1 to n~~

~~T_{sX} – heatsink temperature at a specified surface point~~



Key

T_{vjX} junction temperature of chip X

T_{cX} case temperature under chip X

T_{sX} heat sink temperature under chip X

Figure 6 – Cross-section of an isolated power device with reference points for temperature measurement of T_c and T_s

– Measurement procedure

Cross-sectional view of an isolated power device is shown in Figure 6.

~~T_c~~T_{cX} is measured by a temperature measuring instrument from underneath through a small hole through the heat sink and any thermal interface material underneath the switch X(chip). ~~T_s~~T_{sX} is taken from above at hottest accessible point, nearest to the switch X(chip) or from underneath through a specified sack hole ending at 2 (±1) mm below the heat sink surface (to be specified, type test feature). ~~T_j~~T_{vjX} is determined using indirect methods like described in the individual documents.

~~NOTE~~ The thermal resistance $R_{th(j-s)}$ and $R_{th(c-s)}$ depends on several mechanical parameters such as type and thickness of the used thermal interface material (should be specified in manufacturer's mounting instructions, for example 30 to 50~~µ~~m), the maximum deviation of flatness of the cooling surface of the device's base plate and of the heat sink and the mounting torque of the fixing screws, as per specified mounting instructions.

6.2.4.2 Thermal resistance junction to case per switch (X) $R_{th(j-c)X}$

~~$R_{th(j-c)} = (T_j - T_c)/P$ (2)~~

~~where~~

~~T_j is the virtual junction temperature of the switch;~~

~~T_c is the temperature of the case (base plate) under the switch (chip);~~

~~P is the power dissipation of a switch (see Figure 5).~~

$$R_{th(j-c)X} = (T_{vjX} - T_{cX})/P_X \quad (2)$$

where

X is the D (Diode), T(Thyristor), I (IGBT), M (MOSFET), B(BJT);

T_{vjX} is the virtual junction temperature of the switch X;

T_{cX} is the temperature of the case (base plate) under the switch X(chip);

P_X is the applied power dissipation at the each switch D,T,I,M,B.

Second index might be needed to distinguish multiple devices in one product (e.g., Inverter IGBTs and Brake IGBTs).

6.2.4.3 Thermal resistance case to heat sink per switch (X) $R_{th(c-s)X}$ or per device $R_{th(c-s)}$

~~$R_{th(c-s)(X)} = (T_c - T_s)/P_X$ (3)~~

~~where~~

~~X is the D (Diode), I (IGBT); M (MOSFET)~~

~~T_c is the temperature taken at the specified point of the case (as above) under the chip~~

~~T_s is the temperature of the heat sink, taken at the reference point for testing T_s specified~~

~~P_X is the complete power dissipation of the switch~~

~~P is the power dissipation of the complete device~~

$$R_{th(c-s)X} = (T_{cX} - T_{sX})/P_X \quad (3)$$

where

X is the D (Diode), T(Thyristor), I (IGBT), M (MOSFET), B(BJT);

T_{cX} is the temperature taken at the specified point of the case (as above) under the chip;

T_{sX} is the temperature of the heat sink, taken at the reference point for testing T_s specified;

P_X is the applied power dissipation at the each switch D,T,I,M,B;

P is the whole applied power dissipation of the device.

Second index might be needed to distinguish multiple devices in one product (e.g., Inverter IGBTs and Brake IGBTs).

– Specified conditions
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

NOTE See Annex B for measuring method of the thickness of thermal interface material.

6.2.4.4 Thermal resistance junction to heat sink per switch (X) $R_{th(j\text{-}s)X}$ (for heat sink rated devices)

~~$R_{th(j\text{-}s)} = (T_j - T_{sn})/P$ (4)~~

~~where~~

~~T_j is the virtual junction temperature of the switch;~~

~~T_{sn} is taken at the specified reference point n at the heatsink (see Figure 5);~~

~~P is the power dissipation of the switch.~~

$$R_{th(j\text{-}s)X} = (T_{vjX} - T_{sX})/P_X \quad (4)$$

where

X is the D (Diode), T(Thyristor), I (IGBT), M (MOSFET), B(BJT);

T_{vjX} is the virtual junction temperature of the switch X;

T_{sX} is the temperature of the heat sink, taken at the reference point for testing T_s specified;

P_X is the applied power dissipation at the each switch D,T,I,M,B.

Second index might be needed to distinguish multiple devices in one product (e.g. Inverter IGBTs and Brake IGBTs).

– Specified conditions
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

6.2.4.5 Transient thermal impedance Z_{th}

– Measurement circuit and procedure

These are based on 6.2.4.2 to 6.2.4.4. Individual documents of the non-insulated devices apply.

~~$Z_{th(j-c)} = (|T_j(0) - T_c(0)| - |T_j(t) - T_c(t)|)/P$ (5)~~

~~$Z_{th(c-s)} = (|T_c(0) - T_s(0)| - |T_c(t) - T_s(t)|)/P$ (6)~~

~~$Z_{th(j-s)} = (|T_j(0) - T_s(0)| - |T_j(t) - T_s(t)|)/P$ (7)~~

$$Z_{th(j\text{-}c)X} = (|T_{vjX}(0) - T_{cX}(0)| - |T_{vjX}(t) - T_{cX}(t)|) / P_X \quad (5)$$

$$Z_{th(c\text{-}s)X} = (|T_{cX}(0) - T_{sX}(0)| - |T_{cX}(t) - T_{sX}(t)|) / P_X \quad (6)$$

$$Z_{th(j\text{-}s)X} = (|T_{vjX}(0) - T_{sX}(0)| - |T_{vjX}(t) - T_{sX}(t)|) / P_X \quad (7)$$

– Specified conditions
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement.

7 Acceptance and reliability

7.1 General requirements

In addition to the following subclauses, the requirements applicable to the non-isolated devices as given in the other relevant parts of IEC 60747 apply.

7.2 List of endurance tests

See Table 1.

Table 1 – Endurance tests

Subclause	Environmental testing – designation	Short form	Normative reference
7.2.1	High temperature reverse bias or high temperature blocking	HTRB	IEC 60749-5
7.2.2	High humidity and high temperature reverse bias or high humidity and high temperature blocking	H^3TRB	IEC 60749-5
7.2.3	Power cycling (load) capability		IEC 60749-34
7.2.4	High temperature storage	HTS	IEC 60749-6
7.2.5	Low temperature storage	LTS	IEC 60068-2-~~48~~ [1]1
7.2.6	Thermal cycling	TC	IEC 60749-25
7.2.7	Resistance to solder heat		IEC 60749-15
7.2.8	Solderability		IEC 60749-21
7.2.9	Mechanical shock		IEC 60749-10
7.2.10	Vibration (variable frequency)		IEC 60749-12

~~[1] Withdrawn in 2008.~~

7.3 Acceptance defining criteria

See Table 2.

Table 2 – Acceptance defining characteristics for endurance and reliability tests

Acceptance defining characteristic	Acceptance criteria	Measurement conditions
I_{isol}	< USL	Specified V_{isol}
R_{th}	< USL	Mounting instructions
USL: upper specification limit.		

7.4 Type tests and routine tests

7.4.1 Type tests

The experience which has been obtained with other isolated power semiconductor devices, using the same or similar components such as switches or packages, should be considered when deciding which tests are mandatory.

Type tests are carried out on new products on a sample basis, in order to determine the electrical and thermal and mechanical and climatic ratings (limiting values) characteristics to be given in the data sheet and to establish the test limits for future routine tests. Some or all of the tests should be repeated from time to time on samples drawn from current production or deliveries so as to confirm that the quality of the product continuously meets the requirements.

The minimum type tests to be carried out are as follows.

New isolated power semiconductor devices should undergo the type tests listed in Table 3, marked with "X" (X = mandatory). Some of the type tests are destructive.

Table 3 – Minimum type and routine tests for isolated power semiconductor devices

Subclause	Items	Type test	Routine test	Destructive
5.2.1, 6.1	Isolation voltage (V_{isol}), (V_{isol1})	X	X	
5.2.2, Annex A	Peak case non-rupture current ~~I_{RSMC} ; I_{CNR}~~	X[a]		X
5.3.1	outline dimensions, creepage, clearance	X		
5.3.1.4	flatness of base plate ~~or of cooling surface~~	X	X[b]	
5.3.6, 6.2.4	thermal resistances (R_{th})	X		
5.3.7, 6.2.4.5	transient thermal impedance (Z_{th})	X		
5.3.2, 6.2.2	parasitic inductance (L_p)	X[a]		
5.3.3, 6.2.3	parasitic capacitance (C_p)	X[a]		
5.3.4, 5.3.5, 6.2.1	partial discharge voltages (V_{iM} or $V_{i(RMS)}$) / (V_{eM} or $V_{e(RMS)}$)	X[a]	X[b]	
5.2.5.4	terminal pull-out force (F_t)	X	~~X~~[b]	X
7.2.6[c]	thermal cycling	X		X
7.2.3[c]	power cycling (load)	X		X
7.2.9 [c],7.2.10[c]	mechanical ~~tests~~ shock, vibration	X		X
5.2.6	climatic ~~characteristics classification~~ ratings	X[a]		

NOTE Tests for isolation voltage, partial discharge voltage, creepage and clearance distance should be based on each standard which should be applied to any final equipment using the isolated power semiconductor device. For example, see ~~IEC 60950 (Safety information technology, IEC 61287 (rolling stock)~~ IEC 62368-1, IEC 61287-1, etc.

[a] Type test only for devices with specified maximum values.

[b] Routine test only for devices with specified maximum or minimum values.

[c] See Table 1 for normative references of test.

7.4.2 Routine tests

The routine tests should be carried out on the current production or deliveries normally on a 100 % basis. The ratings and characteristics specified in the data sheet should be verified for each criterion or specimen. Routine test may comprise a selection of the isolated devices into groups of routine tests in Table 3. The minimum routine tests to be carried out on isolated devices are listed in Table 3. Other routine tests are carried out as described in the other parts of the IEC 60747, which is valid for the particular switch.

Annex A
(informative)

Test method of peak case non-rupture current2

A.1 Purpose

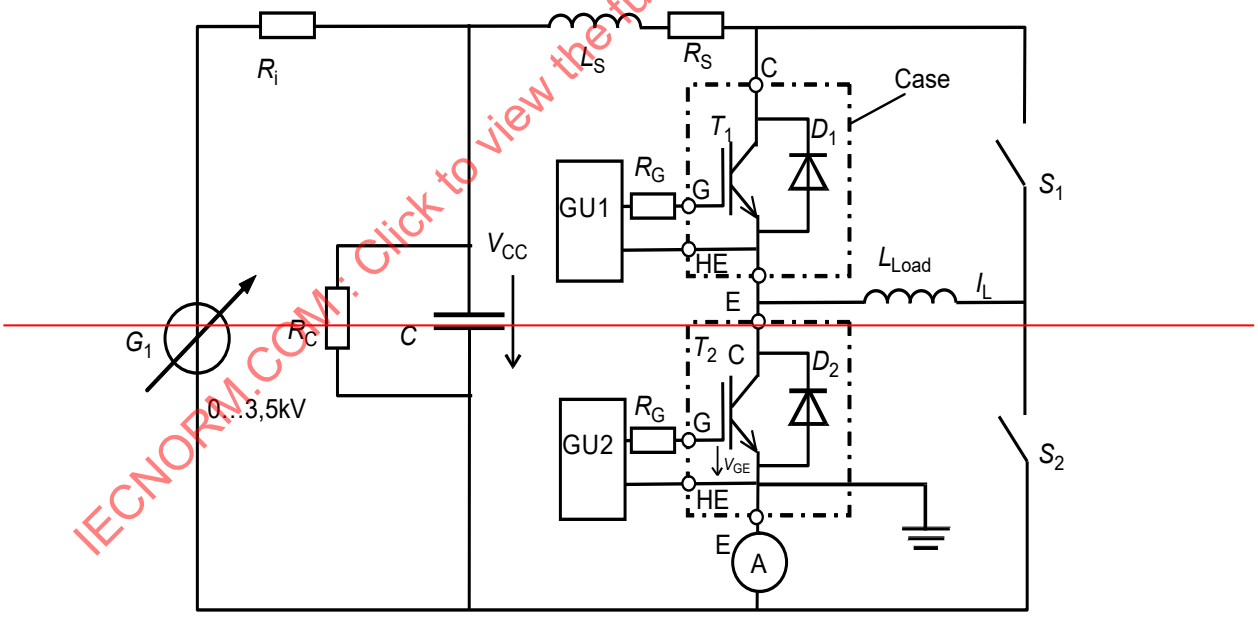
To prove the ability of the isolated power device containing bipolar transistors, IGBTs or MOSFETs as switches to withstand the rated peak case non-rupture current ~~I_{CNR}~~ without causing a rupture (an "explosion") of the case or an emission of plasma beam or ejecting massive particles. This is a destructive test.

~~NOTE 1~~ Case rupture is caused by inside arc or vapour pressure, when the supplied energy or current from outer source exceeds the specified limit. The arc or vapour pressure is induced in a package (encapsulation) of failed power devices by being supplied with stored energy or current from an outer circuit power source. Critical current or energy for packages after the device failure should be issued as an item of the package environmental properties, and in addition the semiconductor and also other electrical parts should avoid an explosion by accident.

NOTE Annex A is applicable if there is an agreement with user.

A.2 Circuit diagram

See Figure A.1.



~~– Circuit description and requirements~~

~~A = Ammeter to measure the device current which can be I_{CNR}, if the case just did not burst, monitored by a current probe having low inductance~~

~~*C* = line capacitor bank, chargeable to full voltage~~

~~D_1 = inverse diode of T_1, high side~~

2 Still under discussion.

~~D_2 = inverse diode of T_2, low side~~

~~G_1 = DC supply voltage source V_{CC}, which can be switched off from mains under all conditions~~

~~GU1 = gate drive unit of T_1~~

~~GU2 = gate drive unit of T_2~~

~~L_{Load} = load inductance~~

~~L_s = parasitic inductance of the circuit (40 nH to 250 nH)~~

~~R_e = discharge resistor for protection purposes~~

~~R_G = gate resistor~~

~~R_i = internal source resistance~~

~~R_s = fuse resistor, mostly set to zero~~

~~S_1 = auxiliary switch (IGBT), high side~~

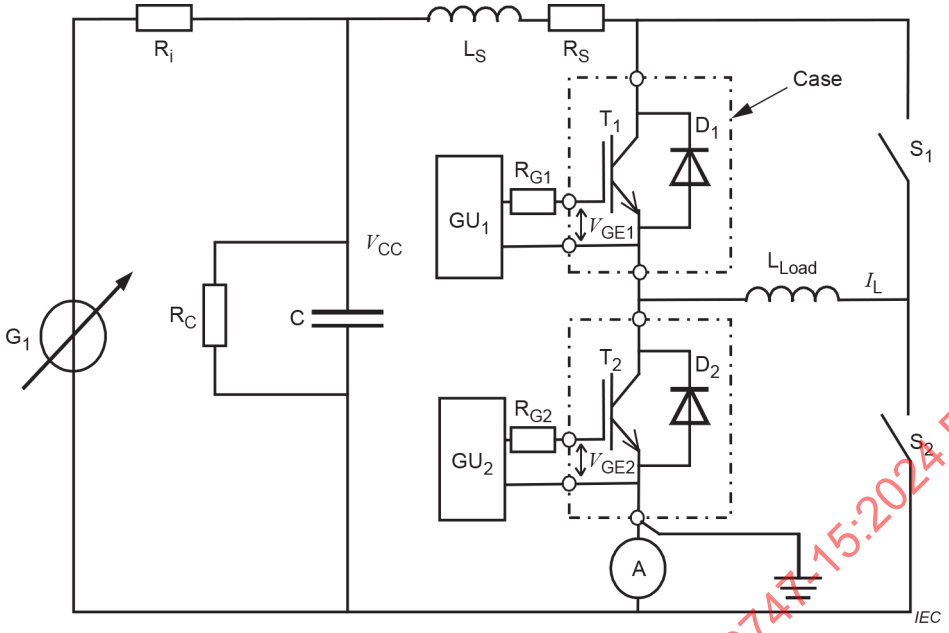
~~S_2 = auxiliary switch (IGBT), low side~~

~~T_1 = high side IGBT switch = device under test (DUT)~~

~~T_2 = low side IGBT switch~~

~~I_L = load current~~

~~V_{GE} = gate voltage~~



Key

A	Ammeter to measure the device current which can be peak case non-rupture current, if the case did not burst, monitored by a current probe having low inductance
C	line capacitor bank, chargeable to full voltage
D_1	inverse diode of T_1, high side
D_2	inverse diode of T_2, low side
G_1	DC supply voltage source V_{CC}, which can be switched off from mains under all conditions
GU_1	gate drive unit of T_1
GU_2	gate drive unit of T_2
L_{Load}	load inductance
L_s	stray inductance of the circuit (specified value)
R_c	discharge resistor for protection purposes
R_{G1}	gate resistor of T_1
R_{G2}	gate resistor of T_2
R_i	internal source resistance
R_s	fuse resistor, mostly set to zero
S_1	auxiliary switch (IGBT), high side
S_2	auxiliary switch (IGBT), low side
T_1	high side IGBT switch = device under test (DUT)
T_2	low side IGBT switch
I_L	load current
V_{GE1}	gate voltage of T_1
V_{GE2}	gate voltage of T_2

Figure A.1 – Circuit diagram for test of peak case non-rupture current ~~I_{CNR}~~

The set-up consists of a two-quadrant converter with two identical isolated IGBT devices. S_1 and S_2 are auxiliary switches, for example IGBT devices, used to establish the desired load current and to induce a short circuit failure. T_1 and T_2 are identical isolated IGBT devices (SINGLE switch or both in a half bridge circuit as DUAL switch). This Annex A describes testing methods using S2.

A.3 Test procedure

- Test A:

  First, close switch S_2, turn on T_1, the load current increases as defined by load inductance L_{Load}. After I_L have exceeded the safe operating area (SOA) for turn-off of T_1, it is attempted to turn off T_1. The initial part of the turn-off process takes place, the current in the device is reduced and part of the current is commuted to the diode D_2. The device T_1 then undergoes a turn-off failure. The diode in the low side device D_2 carries substantial current at this instant. The failure of T_1 forces the diode D_2 to turn off at virtually unlimited di/dt, drawn by L_{Load}. This is outside the diode SOA, and the diode D_2 also fails.

- Test B:

  T_1 is turned on until a substantial load current is reached. At this moment the device T_2 is turned on. It is induced to fail, because it sees the full voltage together with full current. The device T_1 then goes into desaturation and also fails. ~~(Top-bottom shoot-through- which creates a short circuit between plus bus bar and minus bus bar, discharging the capacitor bank, creating an arc in the devices. This leads to production of gases of the surrounding plastic gel etc. until the energy of the capacitor bank is used). In reality such a failure could be due to cosmic ray or due to thermal overload. Manipulating the device can artificially induce it.~~

  ~~Tests C and further tests:~~

These tests are executed until a value of stored energy of the capacitor bank and of peak current is found, which is not high enough to rupture or break the case. The values of achieved peak current I_C = ~~I_{CNR}~~ peak case non-rupture current, V_{CC}, C_{max} and of E_C = ½ CV_{CC}^2 are monitored~~. The value I_{CNR} is the value of a percentage (10 % = 2/20) of a tested population (minimum 10 pieces) of devices, at which the case did not burst, or case split, but did not eject internal particles~~.

A.4 Post test measurements and criteria

The DUT is subjected to a visual test, whether cracks and signs of plasma from arcing inside are visible from outside. There shall be no signs of particles thrown out nor shall there be evidence that the device has externally melted or burst into flames.

~~NOTE 2 The ejection of particles is unavoidable for energies higher than about 10 kJ. What can be achieved by good design is that no massive parts are ejected, which can cause severe consequential damage.~~

A.5 Specified conditions

- Case or virtual junction temperature (T_c = 25 °C, T_{vj} = 25 °C or 125 °C)
- Supply voltage V_{CC}
- Capacitance of capacitor bank C
- Stored energy of capacitor bank E_C
- ~~Parasitic~~Stray inductance of short circuit L_{SC}
- Load current I_L

- Gate voltage V_{GEon} and V_{GEoff}
- Gate resistance R_{Gon} and R_{Goff}
- Percentage of tested devices not burst to total number of tested devices.

NOTE See Bibliography.

Annex B
(informative)

Measuring method of the thickness of thermal compound paste

B.1 General

The measuring gauge is a comb out of stainless ~~steal~~ steel or suitable plastic, which is not solvable by the fluid material of the thickness of layer to be tested. The outer teeth of the comb – those at the edges of the hexagon in Figure B.1 – form a base line. The inner teeth – those between the outer teeth – are progressively shortened, so that a space of distances is achieved between the teeth and the base line. The size of the distance can be read on a scale on the instrument. A typical measuring gauge is shown in Figure B.1.

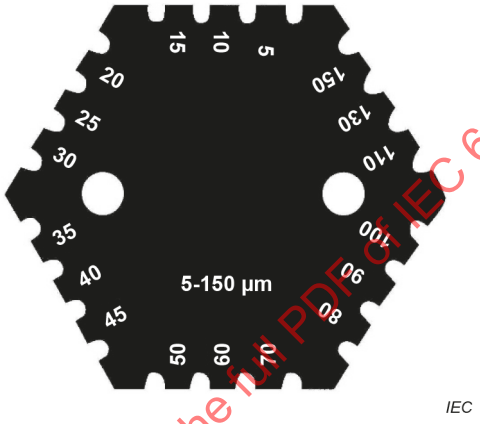


Figure B.1 – Example of a measuring gauge for a layer of thermal compound paste of a thickness between 5 µm and 150 µm

B.2 Measuring method

Immediately after applying the layer, the measuring comb is pressed upon the substrate, so that the teeth are vertical to the surface and the measuring comb does not slip. Remove the comb and look at the teeth to ensure that is the shortest tooth that still touched the fluid layer. The thickness of the layer corresponds to the average mean value of the last touching tooth and the first non-touching tooth. At least two further measurements at different parts on the surface are to be executed in same way to get representative values for the covered area.

This method measures the thickness after grease printing. Therefore, it is very effective for the start-up inspection of the printing type grease application device. However, it is not suitable for inspection of dispenser type grease application equipment or each products warranty, so it is necessary to consider another method for those verifications.

Annex C
(informative)

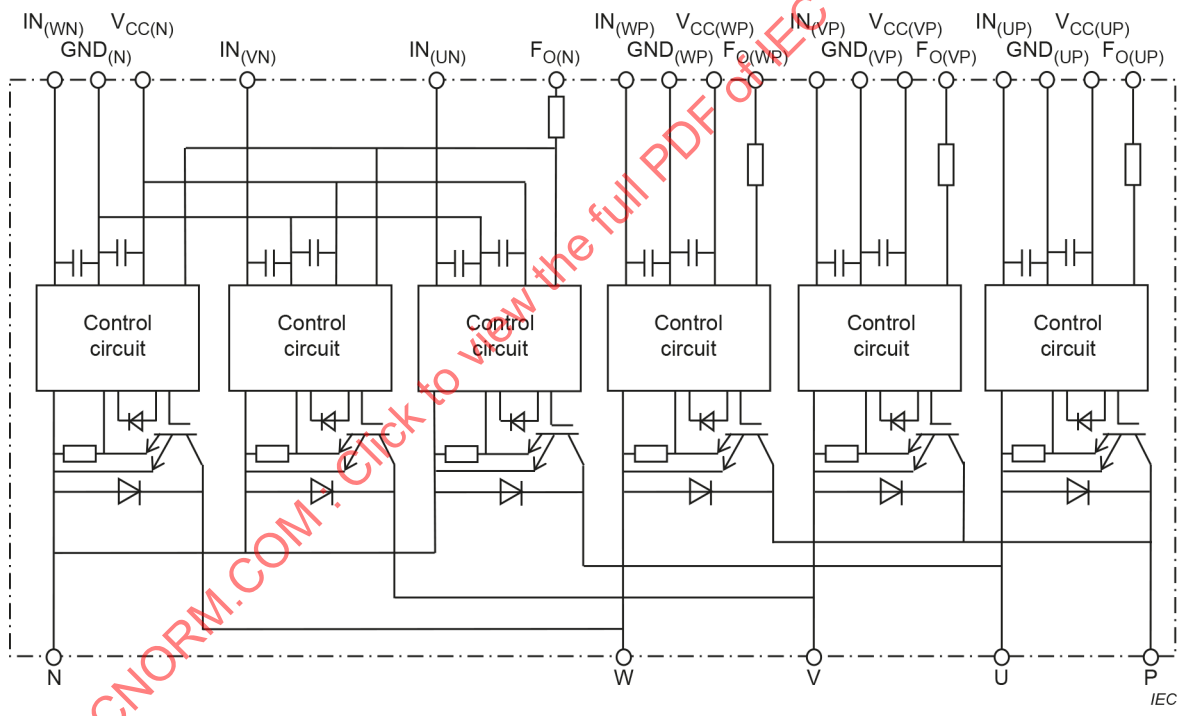
Intelligent power semiconductor modules (IPMs)

C.1 General

Isolated power semiconductor devices are categorized to several type, intelligent power semiconductor module is one of type of them. The intelligent power semiconductor modules (IPMs) include incorporated control circuits, such as gate driving circuit, protection function circuits from abnormal operation. This type of device is widely used in field, this annex shows functions of the IPM as of reference. And IGBT-IPM is used as an example in this annex. Add the descriptions for another type of IPMs if needed in the future.

C.2 Control terminals of IPM

Figure C.1 shows the internal circuit configuration block diagram of representative IPM, main terminals and control terminals.



Key

P	+DC main terminal
N	-DC main terminal
U, V, W	Output main terminals
$V_{CC(UP,VP,WP,N)}$	power supply (+) terminals for control circuits
$GND_{(UP,VP,WP,N)}$	power supply (-) terminals for control circuits / reference potential terminals
$IN_{(UP, VP, WP, UN, VN, WN)}$	input signal terminals of control circuit
$F_{O(UP, VP, WP, N)}$	alarm output terminals of control circuit

Figure C.1 – Example of internal circuit configuration block diagram of IPM

C.3 Essential ratings (limiting value) and characteristics

C.3.1 General

The ratings and characteristics of IPM regarding incorporated control circuit are described in this clause. The input signal for driving the IGBT is low active, that is, the IPM in which the IGBT is turned on when the signal level changes from High to Low is taken as an example. Figure C.1 shows an example of 6 in 1 type IPM that is widely used in the market, but from this section onwards using 2 in 1 type IPM for simplification explain.

NOTE If more than one rating or characteristic names, letter symbols are used in actual application, those are indicated by using "/" as separator.

C.3.2 Ratings (limiting value) and testing method

C.3.2.1 Supply voltage V_D / V_{CC}

Maximum voltage that can be applied between V_{CC} terminal and GND terminal under specified conditions. Both letter symbols V_D and V_{CC} may be used.

C.3.2.2 Input voltage V_{CIN} / Input signal voltage V_{in}

Maximum voltage that can be applied between IN terminal and GND terminal under specified conditions.

C.3.2.3 Fault output voltage V_{FO} / Alarm signal voltage V_{ALM}

Maximum voltage that can be applied between F_O terminal and GND terminal under specified conditions.

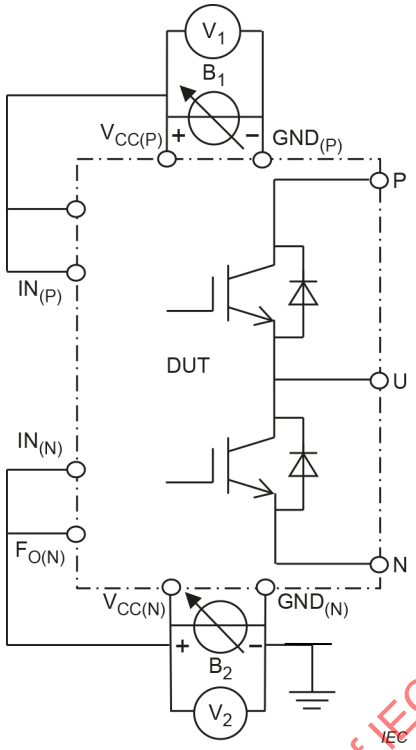
Testing method for the above three ratings is shown below.

– Purpose

  To confirm that there is no abnormality when the rated voltage of the control circuit is applied to the control circuit of the DUT under the specified conditions.

– Test circuit

  Testing circuit is shown in Figure C.2, as an example of 2 in1 type IPM.



Key

DUT IPM under test

B_1 Power supply voltage source of upper arm control circuit

B_2 Power supply voltage source of lower arm control circuit

V_1 Voltmeter for upper arm control circuit power supply observation

V_2 Voltmeter for lower arm control circuit power supply observation

Figure C.2 – Testing circuit for supply voltage, input voltage / input signal voltage, and fault output voltage / alarm signal voltage

– Test procedure

1) Connect the test circuit shown in Figure C.2 to the DUT.
2) Set the DUT to the specified temperature by a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_1, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_2.
4) Confirm that there are no abnormalities after the test.

– Specified conditions

a) Voltage of control circuit power supply B_1, B_2.
b) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.2.4 Fault output current I_{FO} / Alarm signal current I_{ALM}

Maximum current that can be flown between F_O terminal and GND terminal under specified conditions.

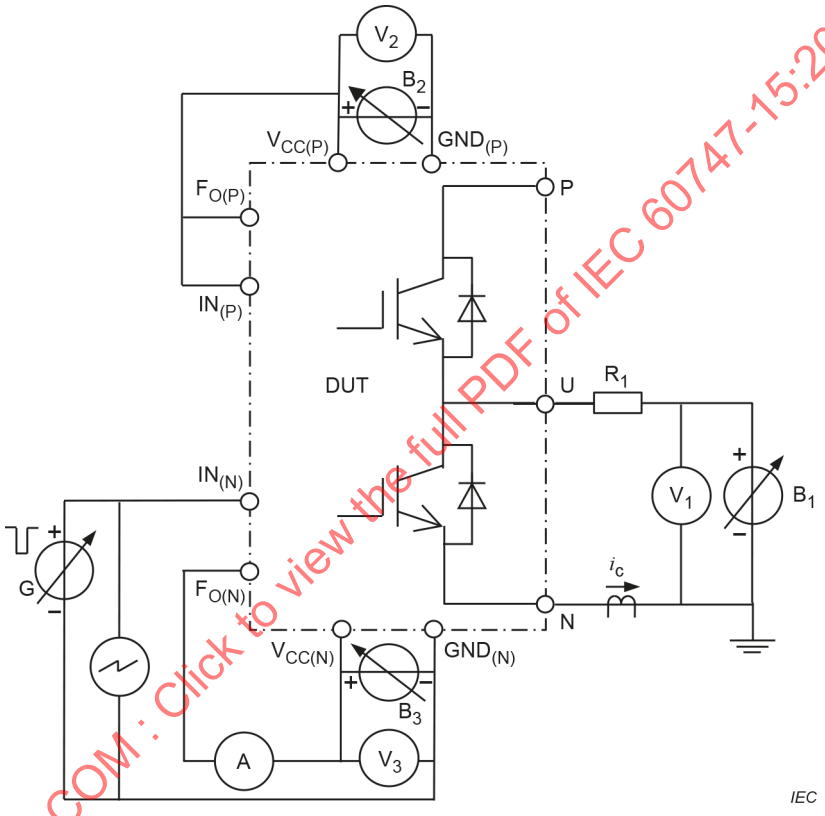
Testing method is shown below.

– Purpose

To confirm that there is no abnormality when the rated current of the control circuit is applied to the DUT control circuit under the specified conditions.

– Test circuit

Testing circuit is shown in Figure C.3.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for collector current power supply observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
OSC	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation
R_1	Current limiting resistor
A	Ammeter for fault output current observation

Figure C.3 – Testing circuit for fault output current / alarm signal current

– Test procedure

1) Connect the test circuit shown in Figure C.3 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the ON-signal between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by the Variable pulse voltage source G.
5) Increase the voltage of the power supply voltage source B_1 until over current protection / short circuit protection function is activated.
6) When the over current protection / short circuit protection is activated, observe the current flowing to the $F_{O(N)}$ terminal with an ammeter (or current sensor with oscilloscope) and confirm that it can withstand the rated current.
7) Confirm that there are no abnormalities after the test.

– Specified conditions

a) Collector current of over current protection / short circuit trip level;
b) Specified current I_{FO} or I_{ALM} to $F_{O(N)}$ terminal (adjustable by B_3 voltage);
c) Voltage of control circuit power supply B_2, B_3;
d) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
e) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.2.5 Main circuit DC bus voltage at short circuit V_{SC}

Maximum DC bus voltage of the main circuit (voltage between the P terminal and the N terminal of the IPM) that can perform protective operation in the event of a short circuit when the specified test set temperature and specified control voltage are applied.

If a short circuit occurs at a voltage exceeding this value, protection cannot be performed, and the device may be destroyed.

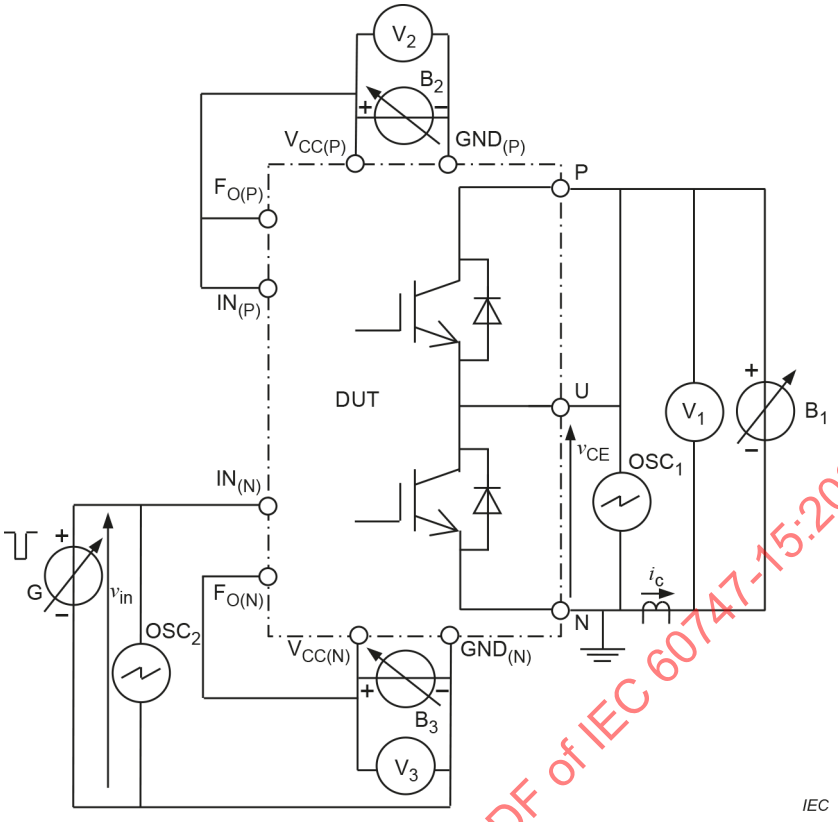
Testing method is shown below.

– Purpose

To confirm that the DUT is protected by the protection function in the event a short circuit and can withstand the short circuit protection operation under the specified conditions.

– Test circuit

Testing circuit is shown in Figure C.4, and the waveforms are shown in Figure C.5.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
OSC_1	Oscilloscope for voltage v_{CE} between collector and emitter observation
OSC_2	Oscilloscope for voltage v_{in} between $IN_{(N)}$ and $GND_{(N)}$ observation

Figure C.4 – Testing circuit for main circuit DC bus voltage at short circuit

– Test procedure

1) Connect the test circuit shown in Figure C.4 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3. Also, apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
4) Apply the ON-signal (longer enough to activate short circuit protection, usually 10 µs or more) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by the Variable pulse voltage source G.
5) Confirm that there are no destruction or abnormalities after the short circuit test.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;

b) Specified main DC bus voltage (between P and N terminal by voltage source B_1);

c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;

d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

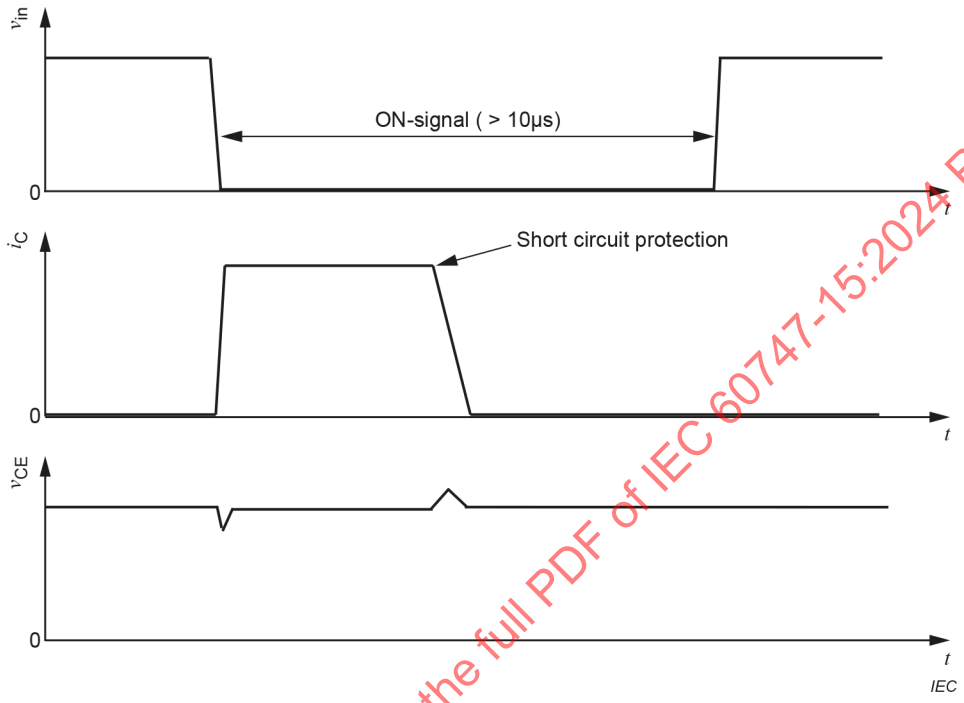


Figure C.5 – Waveforms of short circuit protection function

C.3.2.6 Acceptance defining criteria

All rating tests should be verified to be normal by measuring the characteristics of the IPM control circuit shown in Table C.1 after the tests are completed. The normal characteristic value is not higher than the upper limit USL of the acceptance criteria and is not lower than the lower limit LSL.

Table C.1 – Acceptance defining criteria for the IPM control circuit after rating tests

Subclause	Acceptance defining characteristics	Acceptance criteria
C.3.3.5	Short circuit trip level SC / Over current protection level I_{OC}	SC / I_{OC} > LSL
C.3.3.8	Control circuit under-voltage protection UV / V_{UV}	LSL < UV / V_{UV} < USL
C.3.3.3	Control circuit current I_D / I_{CCP}, I_{CCN}	I_D / I_{CCP}, I_{CCN} < USL
USL: upper specified limit. LSL: lower specified limit.		

C.3.3 Characteristics and measuring method

C.3.3.1 Turn-off times and turn-off switching energy at inductive load

Turn-off times and turn-off switching energy of IPM are defined with starting from the time when the input threshold voltage reached, under the specified measurement set temperature and specified control circuit conditions.

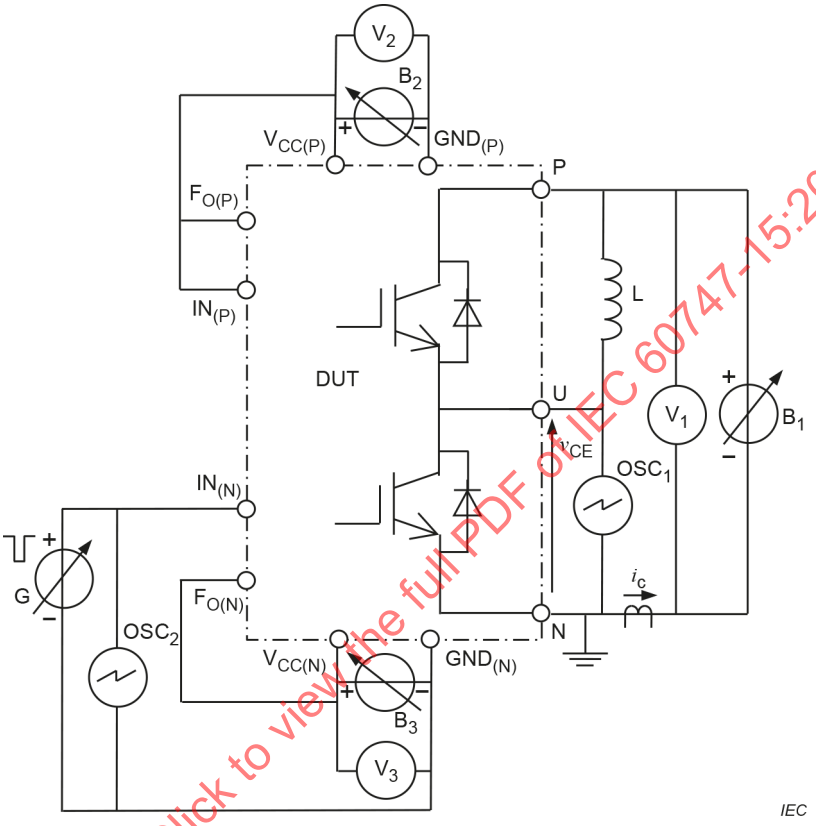
Measurement method is shown below.

– Purpose

To measure the turn-off switching times and turn-off switching energy when an inductive load current is passed through the DUT under the specified conditions.

– Measurement circuit

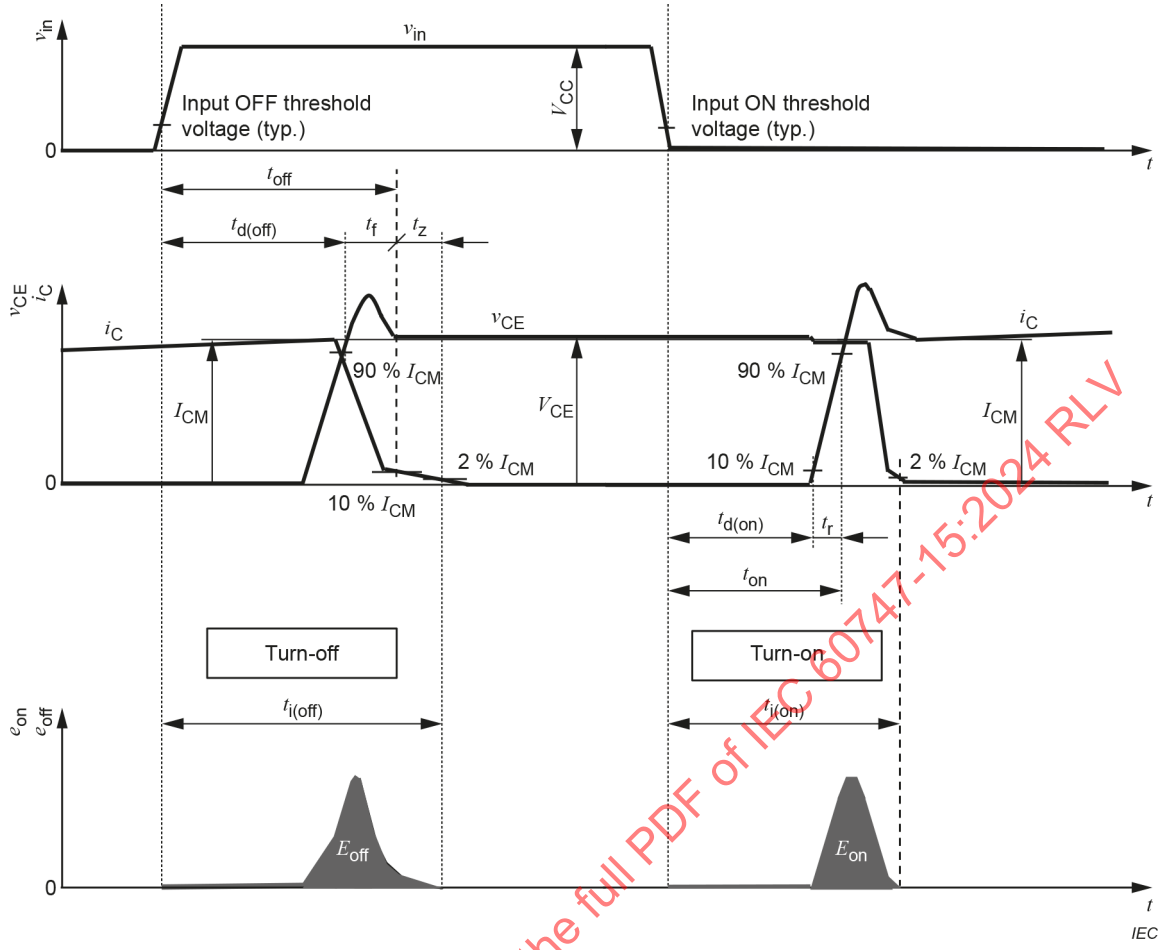
Measurement circuit is shown in Figure C.6, and the waveforms are shown on left side of Figure C.7.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
L	Load inductor
OSC_1	Oscilloscope for voltage between collector and emitter observation
OSC_2	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

Figure C.6 – Measurement circuit for switching times and switching energy at inductive load (lower arm device measurement)



Key

$t_{d(off)}$	Turn-off delay time	$t_{d(on)}$	Turn-on delay time
t_f	Fall time	t_r	Rise time
t_z	Tail time	t_{off}	Turn-off time
E_{off}	Turn-off energy	t_{on}	Turn-on time
$t_{i(off)}$	Integral time for turn-off energy	E_{on}	Turn-on energy
		$t_{i(on)}$	Integral time for turn-on energy

Figure C.7 – Switching waveforms at inductive load

– Measurement procedure

1) Connect the test circuit shown in Figure C.6 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G in order to turn on the IGBT of DUT for the specified period. Adjust the voltage of the variable constant voltage power supply B_1 to raise the collector current flowing through the load inductor L to the specified current. Then, turn off the IGBT to observe the waveforms of the $IN_{(N)}$ terminal and $GND_{(N)}$ terminal voltage v_{in}, collector-emitter voltage v_{CE}, and collector current i_C with the oscilloscope and current sensor.

5) From the observed waveform, find the switching times at turn-on ($t_{d(off)}$, t_f, t_z, t_{off}) shown in Figure C.7, and calculate turn-on switching energy E_{off} which is integrated the product of the collector-emitter voltage v_{CE} and the collector current i_C over the integral time $t_{i(off)}$.

– Specified conditions

a) Collector current I_{CM};

b) Voltage of control circuit power supply B_2, B_3;

c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;

d) Specified main DC bus voltage (between P and N terminal by voltage source B_1);

e) Inductance value of the load inductor L;

f) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.2 Turn-on times and turn-on switching energy at inductive load

Turn-on times and turn-on switching energy of IPM are defined with starting from the time when the input threshold voltage reached, under the specified measurement set temperature and specified control circuit conditions.

Measurement method is shown below.

– Purpose

To measure the turn-on switching times and turn-on switching energy when an induced load current is passed through the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.7, and the waveforms are shown on right side of Figure C.7.

– Measurement procedure

1) Connect the test circuit shown in Figure C.6 to the DUT.

2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.

3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.

4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G in order to turn on the IGBT of DUT for the specified period. Adjust the voltage of the variable constant voltage power supply B_1 to raise the collector current flowing through the load inductor L to the specified current. Turn off the IGBT once and circulate the current through the load inductor L and the freewheeling diode on the opposite arm. Then, turn on the IGBT again by applying second ON-signal pulse in order to observe the waveforms of the $IN_{(N)}$ terminal and $GND_{(N)}$ terminal voltage v_{in}, collector-emitter voltage v_{CE}, and collector current i_C with the oscilloscope and current sensor.

5) From the observed waveform, find the switching times at turn-on ($t_{d(on)}$, t_r, t_{on}) shown in Figure C.7, and calculate turn-on switching energy E_{on} which is integrated the product of the collector-emitter voltage and the collector current i_C over the integral time $t_{i(on)}$.

NOTE By measuring the voltage and current waveforms of the opposite (upper) arm at the time of inductive load turn-on, the reverse recovery time, reverse recovery loss energy, and reverse recovery charge of the freewheeling diode can be measured.

– Specified conditions

a) Collector current I_{CM};

b) Voltage of control circuit power supply B_2, B_3;

c) Specified input signal (double pulse) between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;

d) Specified main DC bus voltage (between P and N terminal by voltage source B_1);

e) Inductance value of the load inductor L;

f) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.3 Control circuit current of upper arm I_D / I_{CCP}, and control circuit current of lower arm I_D / I_{CCN}

The maximum value of the effective current consumed by the control circuit of the IPM in the specified measurement set temperature, the specified control circuit conditions, and the input signal is off or the drive signal to the IGBT is input at the specified frequency.

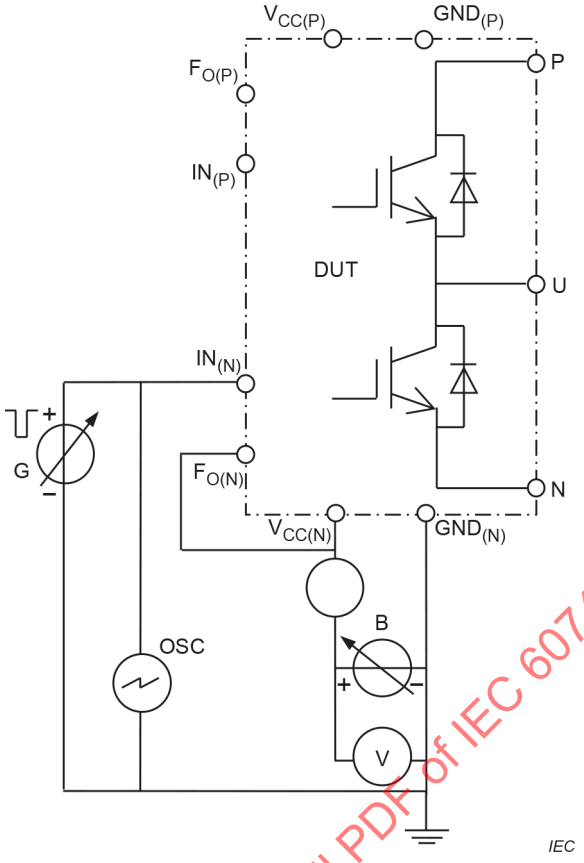
Measurement method as example of lower arm is shown below.

– Purpose

To measure the control circuit current of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.8.



Key

DUT IPM under test

G Variable pulse voltage source

B Power supply voltage source of lower arm control circuit

OSC Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

V Voltmeter for lower arm control circuit power supply observation

A Ammeter for lower arm control circuit power supply observation

Figure C.8 – Measurement circuit for control circuit current

– Measurement procedure

1) Connect the test circuit shown in Figure C.8 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal by the power supply voltage source B, and apply the input signal between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G.
4) Measure the control circuit current by ammeter A.

– Specified conditions

a) Voltage of control circuit power supply B;
b) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.4 Input ON threshold voltage $V_{th(on)}$ / $V_{inth(on)}$, and input OFF threshold voltage $V_{th(off)}$ / $V_{inth(off)}$

Maximum, minimum and typical values of the input ON / OFF threshold voltage to the control circiot for outputting the ON / OFF signal to the IGBT under the specified measurement set temperature and specified control circuit conditions.

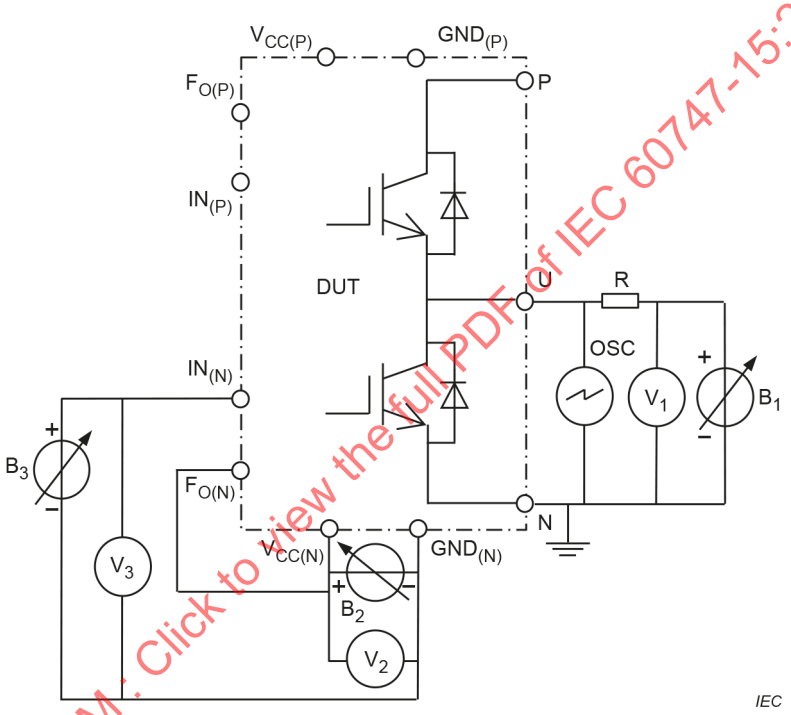
Measurement method as example of lower arm is shown below.

– Purpose

To measure the input ON threshold voltage and input OFF threshold voltage of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.9.



Key

DUT IPM under test

B_1 Power supply voltage source for collector current

B_2 Power supply voltage source of lower arm control circuit

B_3 Voltage source between $IN_{(N)}$ and $GND_{(N)}$

V_1 Voltmeter for main DC bus voltage (between P terminal and N terminal) observation

V_2 Voltmeter for lower arm control circuit power supply observation

V_3 Voltmeter for lower arm input signal observation

R Current limiting resistor

OSC Oscilloscope for voltage between collector and emitter observation

Figure C.9 – Measurement circuit for input threshold voltage

– Measurement procedure for input ON threshold voltage

1) Connect the test circuit shown in Figure C.9 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal by the power supply voltage source B_2.
4) Decrease voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal gradually, then, measure the voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by voltmeter V_3 when collector-emitter voltage go down to specified value.

– Measurement procedure for input OFF threshold voltage

After measurement of input ON threshold voltage, increase voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal gradually, then, measure the voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by voltmeter V_3 when collector-emitter voltage go up to voltage of B_1.

– Specified conditions

a) Voltage of B_1 for collector current supplying;
b) Voltage of control circuit power supply B_2;
c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.5 Over current protection level I_{OC} / Short circuit trip level SC

Minimum trip level for over current protection or short-circuit protection under the specified measurement set temperature and specified control circuit conditions.

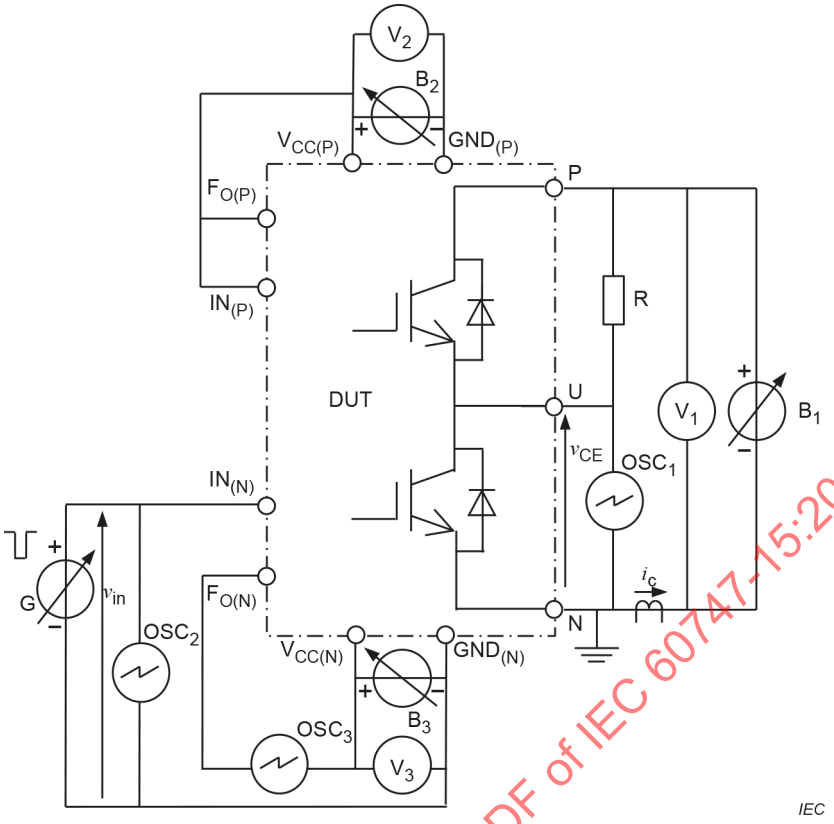
Measuring method as example of lower arm is shown below.

– Purpose

To measure the over current protection level / short circuit trip level of the DUT under the specified conditions.

– Measurement circuit

Measuring circuit is shown in Figure C.10, and waveforms during the protection operation are shown in Figure C.11.



Key

DUT IPM under test

B_1 Power supply voltage source for collector current

B_2 Power supply voltage source of upper arm control circuit

B_3 Power supply voltage source of lower arm control circuit

V_1 Voltmeter for main DC bus voltage (between P terminal and N terminal) observation

V_2 Voltmeter for upper arm control circuit power supply observation

V_3 Voltmeter for lower arm control circuit power supply observation

G Variable pulse voltage source

R Load resistor

OSC_1 Oscilloscope for voltage between collector and emitter observation

OSC_2 Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

OSC_3 Oscilloscope for Fault / Alarm output signal observation

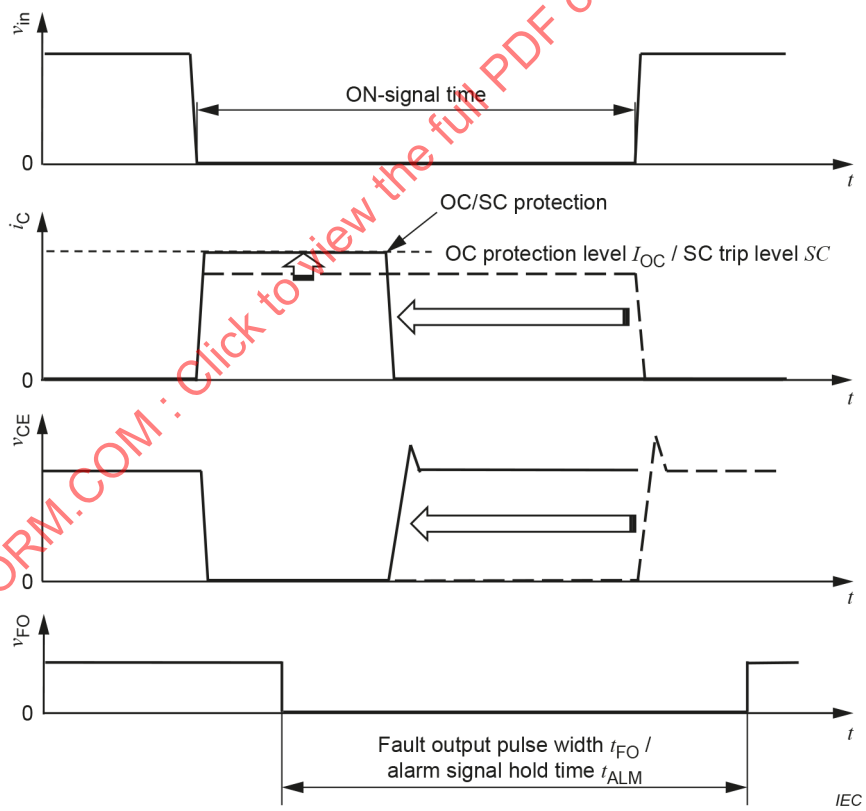
Figure C.10 – Measuring circuit for over current protection level/short circuit trip level

– Measurement procedure for input ON threshold voltage

1) Connect the test circuit shown in Figure C.10 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G, and increase gradually the voltage of the variable constant voltage power supply B_1 to raise the collector current until the protection function operation.
5) Then, measure the collector current just before protection operation, fault output pulse width or alarm time, and fault or alarm output signal v_{FO} simultaneously.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;
b) Input ON-signal (longer enough than t_{dOC} / $t_{off(SC)}$);
c) Voltage of B_1 for collector current supplying (< V_{SC}) with adjusting R_0;
d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.



NOTE The fault or alarm output signal can be measured by current I_{FO} observation like Figure C.3 or current sensor with oscilloscope instead of voltage v_{FO} observation. In that case, the i_{FO} waveform is inverse shape of v_{FO}.

Figure C.11 – Waveforms during over current protection / short circuit protection

C.3.3.6 Over current protection delay time t_{doc} / Short circuit current delay time $t_{off(SC)}$

Typical value of collector turn-off delay time during over current protection or short circuit protection operation under the specified measurement set temperature and specified control circuit conditions.

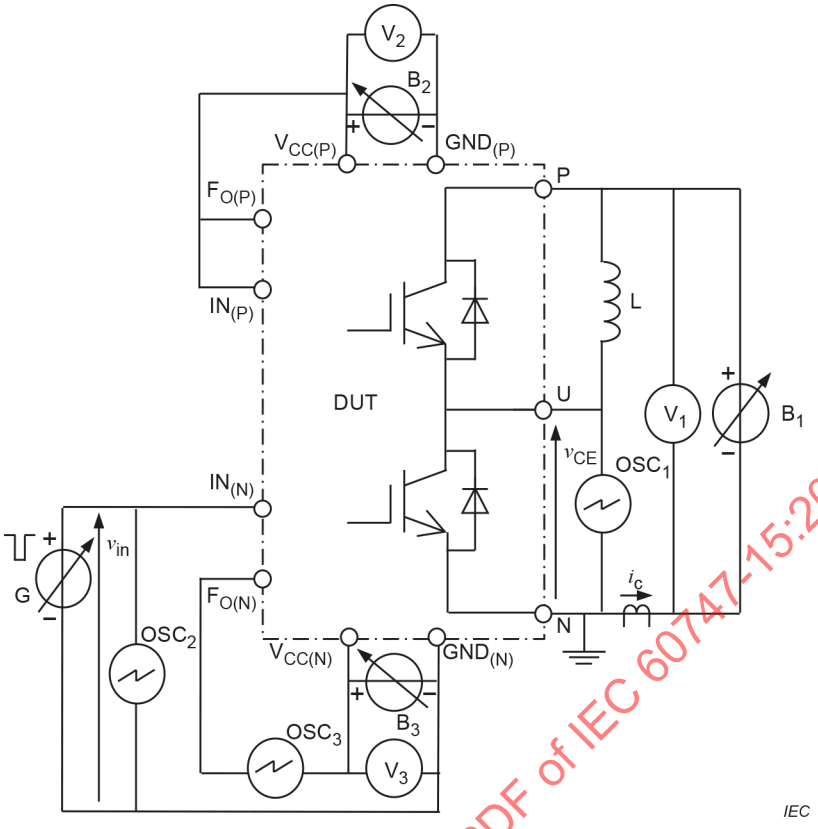
Measurement method as example of lower arm is shown below.

– Purpose

To measure the over current protection delay time t_{dOC} / short circuit current delay time $t_{off(SC)}$ of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.12, and waveforms during the protection operation are shown in Figure C.13.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
L	Load inductor
OSC_1	Oscilloscope for voltage between collector and emitter observation
OSC_2	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation
OSC_3	Oscilloscope for fault / alarm output signal observation

Figure C.12 – Measurement circuit for over current protection delay time/Short circuit current delay time

– Measurement procedure

1) Connect the test circuit shown in Figure C.12 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
5) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G, and increase gradually the ON-signal pulse width to raise the collector current until the protection function operation.
6) Then, measure the time from when the over current protection level or the short circuit trip level is exceeded until the fault output signal starts to be output.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;
b) Specified main DC bus voltage (between P and N terminal by voltage source B_1);
c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

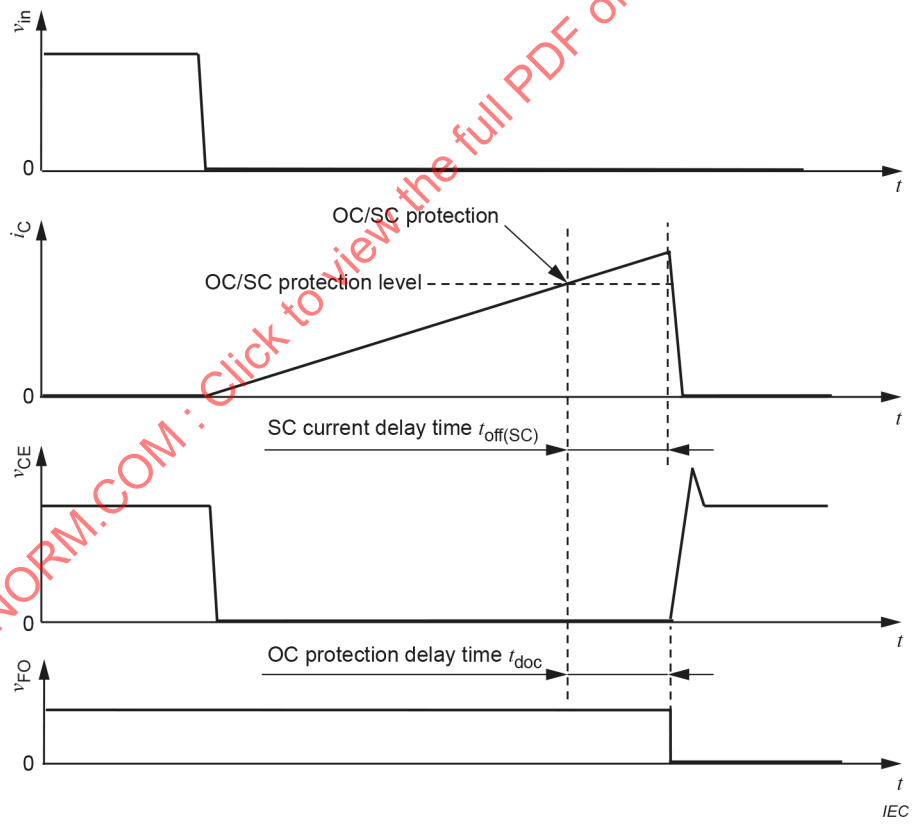


Figure C.13 – Waveforms of protection delay time during over current protection / short circuit protection

C.3.3.7 Over temperature protection OT / overheating protection temperature level T_{jOH}, and over temperature protection hysteresis $OT_{(hys)}$ / overheating protection hysteresis T_{jH}

Typical or minimum value of the over temperature protection level or overheating protection trip level, and the over temperature protection hysteresis or overheating protection hysterisis under the specified measurement set temperature and specified control circuit conditions.

Measurement method as example of lower arm is shown below.

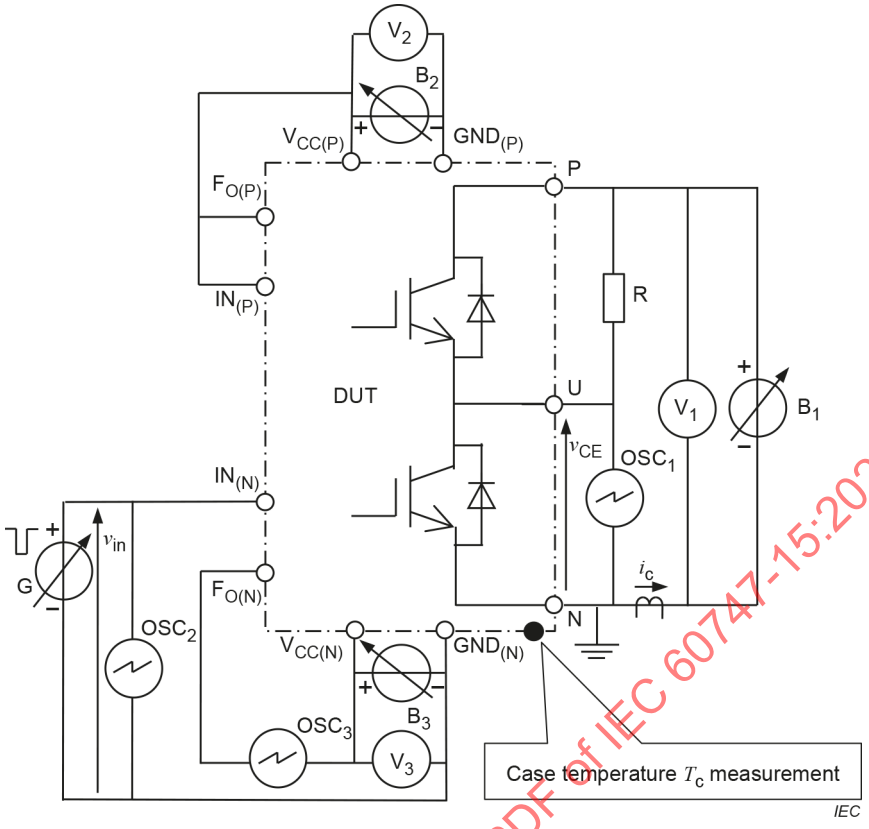
– Purpose

To measure the over temperature protection OT / overheating protection temperature level T_{jOH}, and the over temperature protection hysteresis $OT_{(hys)}$ / overheating protection hysteresis T_{jH} of the DUT under the specified conditions.

The thermal protection trip level and reset level measurement exceeds the maximum rated junction temperature, so the product structure may be destroyed.

– Measurement circuit

Measurement circuit is shown in Figure C.14, and waveforms during the protection operation are shown in Figure C.15.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
R	Load resistor
OSC_1	Oscilloscope for voltage between collector and emitter observation
OSC_2	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation
OSC_3	Oscilloscope for fault / alarm output signal observation

Figure C.14 – Measurement circuit for over temperature protection and its hysteresis

– Measurement procedure

1) Connect the test circuit shown in Figure C.14 to the DUT.
2) Set the DUT on a hot plate or constant temperature chamber with large enough heat capacity enable to adjust case temperature.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
5) Input the ON / OFF signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G, and set the collector current value (pulse width duty) sufficiently small so that the virtual junction temperature does not rise.
6) Adjust setting of the hot plate or constant temperature chamber to raise the case temperature T_c slowly (dT/dt is 1 °C/min. or around), and measure the case temperature when the collector current is cut off or a fault output signal is output. The frequency of the input signal is short enough for the case temperature Tc changes, the guideline is 1 Hz or around.
7) After measuring the over temperature protection or overheating protection temperature level, lower the case temperature T_c slowly (dT/dt is 1 °C/min. or around), and measure the case temperature when the collector current flows again. The difference between this temperature and the over temperature protection or overheating protection temperature level is the overheating protection hysteresis $OT_{(hys)}$ / T_{jH}.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;
b) Main DC bus voltage (between P and N terminal by voltage source B_1);
c) Temperature of the hot plate or constant temperature chamber (the temperature is raised up until overheat protection function is activated);
d) Collector current.

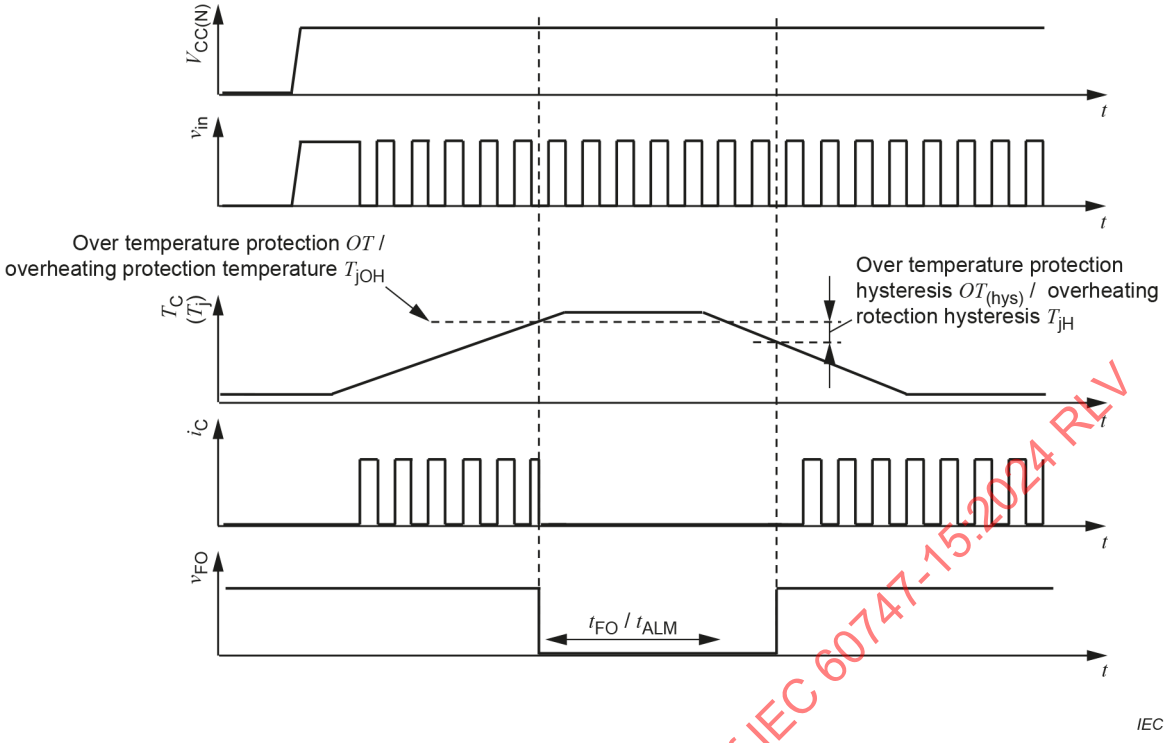


Figure C.15 – Waveforms during the overheating protection operation and the fault output

C.3.3.8 Control circuit under-voltage protection UV / Under-voltage protection level V_{UV}, control circuit under-voltage protection reset level UV_r / Under-voltage protection hysteresis V_H, and fault output pulse width t_{FO} / alarm signal hold time t_{ALM}

Maximum, minimum and typical values of the control circuit under-voltage protection trip level, the control circuit under-voltage protection reset level or the control circuit under-voltage protection hysteresis, and the fault output pulse width or the alarm signal hold time under the specified measurement set temperature and specified control circuit conditions.

Measurement method as example of lower arm is shown below.

– Purpose

  To measure the control circuit under-voltage protection trip level, reset level or protection hysteresis, and fault output pulse width or alarm signal hold time of the DUT under the specified conditions.

– Measurement circuit

  Measurement circuit is same as shown in Figure C.10, and waveforms during the protection operation are shown in Figure C.16.

– Measurement procedure

1) Connect the test circuit shown in Figure C.10 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
5) Input the ON / OFF signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G and set the collector current value (pulse width duty) sufficiently small so that the virtual junction temperature does not rise.
6) Decrease voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ slowly from specified value, and measure the control circuit power supply voltage by voltmeter V_3 when the collector current is cut off or a fault output signal is output. The frequency of the input signal is short enough for the voltage changes of B_3.
7) After measuring the under-voltage protection trip level, increase the voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ slowly, and measure the control circuit power supply voltage (reset level) by voltmeter V_3 when the collector current flows again.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3 (the voltage of B_3 is decreased until protection function is activated);
b) Main DC bus voltage (between P and N terminal by voltage source B_1);
c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj};
d) Collector current.

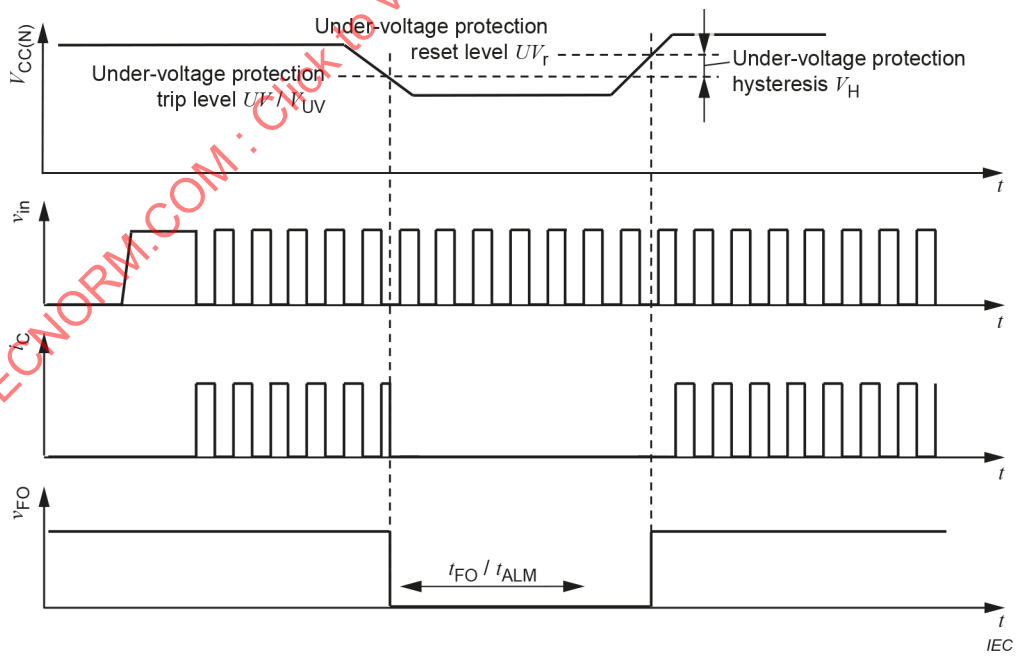


Figure C.16 – Waveforms during the under-voltage protection operation and the fault output

C.3.3.9 Fault output current $I_{FO(H)}$ (during unprotection), $I_{FO(L)}$ (during protection), and alarm signal current limiting resistance value R_{ALM}

Maximum and typical values of the fault output current during no protection operation and the fault output current during the protection operation under the specified measurement set temperature and specified control circuit conditions.

The fault or alarm output signal current $I_{FO(L)}$ is typical or maximum value usually. On the other hand, the fault or alarm output signal current during no protection function operation is expressed with letter symbol of $I_{FO(H)}$, maximum value is required usually.

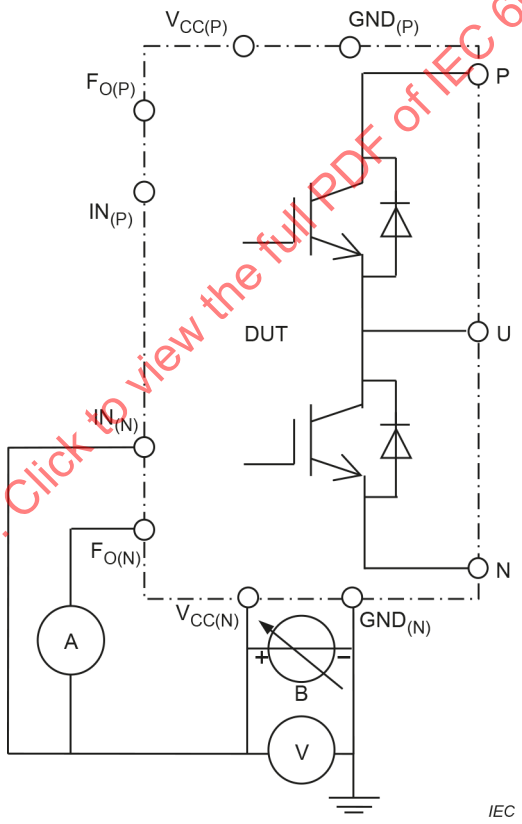
Measurement method as example of lower arm is shown below.

– Purpose

To measure the fault output current $I_{FO(H)}$, $I_{FO(L)}$, and the alarm signal current limiting resistance value R_{ALM} of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.17.



Key

DUT IPM under test

B Power supply voltage source of lower arm control circuit

V Voltmeter for lower arm control circuit power supply observation

A Ammeter for fault/alarm output current

Figure C.17 – Measurement circuit for fault output current

– Measurement procedure

1) Connect the test circuit shown in Figure C.17 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal, and measure the $I_{FO(H)}$ current flowing through the $F_{O(N)}$ terminal by ammeter A or current sensor with oscilloscope. Since the fault output current $I_{FO(L)}$ is the current during the protection operation, it is measured during the over current protection level / short circuit trip level measurement. See C.3.3.5. Use an ammeter or current sensor with oscilloscope instead of OSC_3 in Figure C.10.
4) Since the alarm signal current limiting resistance value R_{ALM} is not measured directly, it is calculated by the control circuit power supply voltage value (voltage value of B) divided by the fault output current $I_{FO(L)}$.

– Specified conditions

a) Voltage of control circuit power supply B;
b) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.10 Common mode noise withstand capability

Maximum or typical allowable noise withstand capability that does not malfunction with respect to common mode noise to commercial input power supplies.

Measurement method as example of lower arm is shown below.

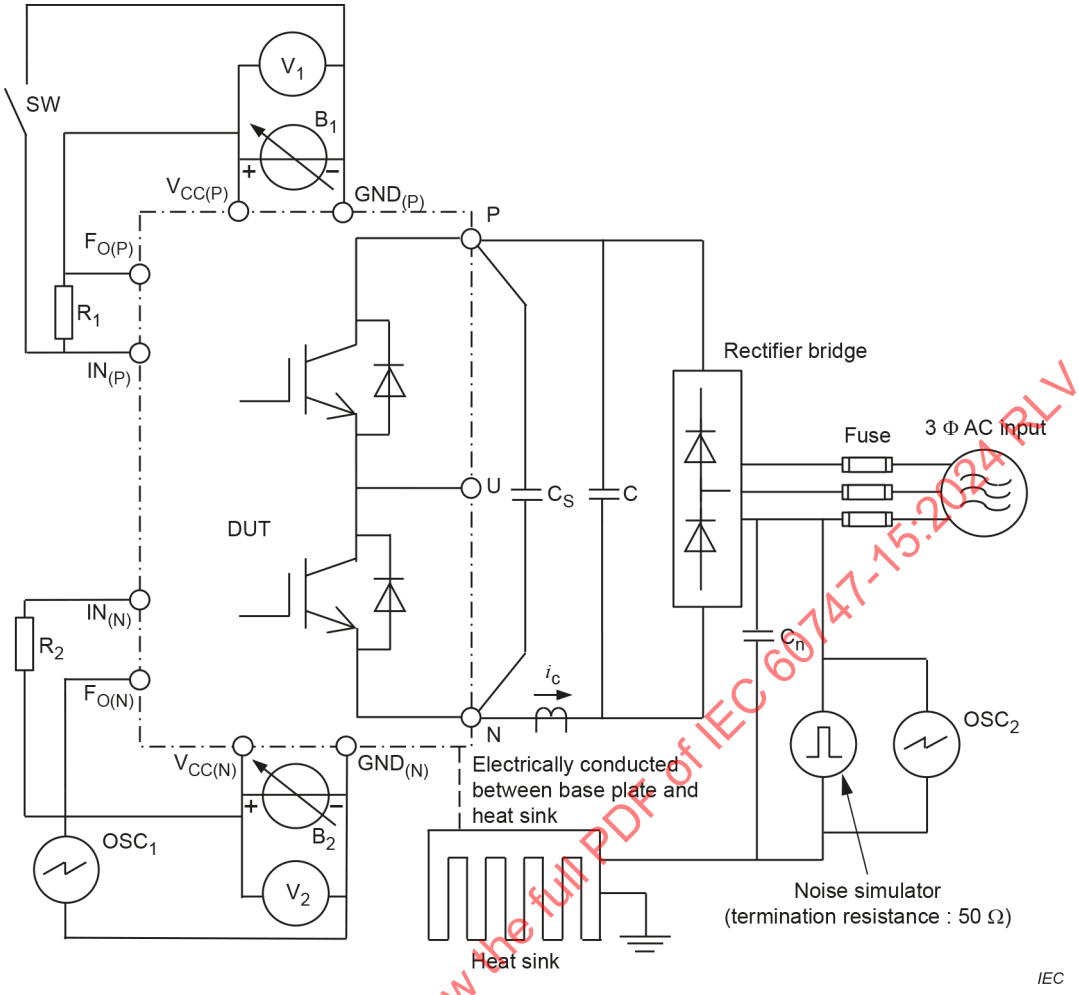
– Purpose

To measure the noise withstand capability of the common mode noise voltage applied to the commercial input power supply so that the DUT does not erroneously turn on or output fault signal under the specified conditions.

NOTE If the IPM operates incorrectly, it can cause a major obstacle, such as a short circuit accident. On the other hand, even if the IPM erroneously turns off, it recovers when the input PWM signal is turned off, and in many cases it does not pose a critical obstacle to the load output. Therefore, the description of the measurement method for erroneous off is omitted.

– Measurement circuit

Measurement circuit is shown in Figure C.18, and waveforms during the operation are shown in Figure C.19. The control circuit of the upper arm that are not measured are always ON, and the lower arm to be measured is always OFF. Also, both ends of the DC bus capacitor C_P and the snubber capacitor C_S are connected to the P and N terminal of the DUT.



Key

DUT	IPM under test
B_1	Power supply voltage source of upper arm control circuit
B_2	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for upper arm control circuit power supply observation
V_2	Voltmeter for lower arm control circuit power supply observation
R_1	Upper arm input signal pull-up resistor
R_2	Lower arm input signal pull-up resistor
SW	ON fixing switch
C	DC bus capacitor
C_S	Snubber capacitor
Cn	Grounding capacitor
OSC_1	Oscilloscope for lower arm control circuit fault output observation
OSC_2	Oscilloscope for noise voltage waveform observation

Figure C.18 – Measurement circuit for common mode noise withstand capability

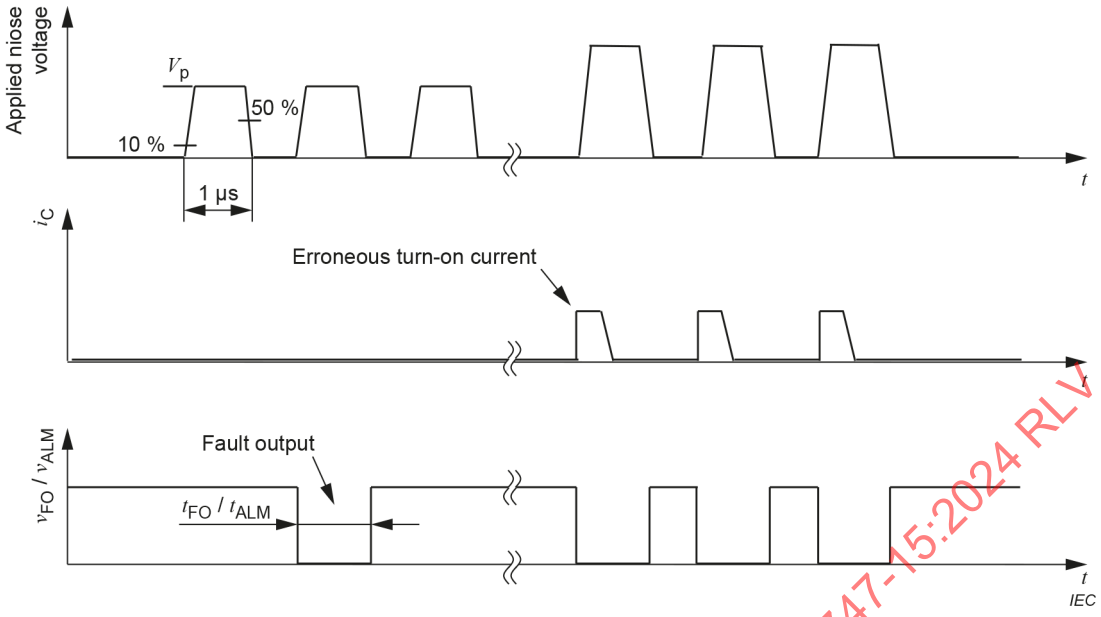


Figure C.19 – Waveforms during the common mode noise withstand capability measurement

– Measurement procedure

1) Pull up the $IN_{(N)}$ terminal to $V_{CC(N)}$ through the pull-up resistor R_2 so that the lower arm of the DUT does not turn on. The pull-up resistor shall have a resistance value equivalent to that in actual use. Usually, 20 kΩ or around is often used.
2) Pull up the $IN_{(P)}$ terminal to $V_{CC(P)}$ through the pull-up resistor R_1 so that the upper arm of the DUT turns on always. Also, pull up the $F_{O(P)}$ terminal of the upper arm to $V_{CC(P)}$ to prevent malfunction. Provide a circuit to turn on with the switch SW.
3) For the upper arm control circuit power supply voltage source B_1 and the lower arm control circuit power supply voltage source B_2, use isolation transformers or the like to reduce stray capacitance to ground, and set them to the specified values $V_{CC(P)}$ and $V_{CC(N)}$, respectively. Insulate the oscilloscope OSC_1 and OSC_2 with isolation transformers or the like as well.
4) Turn on the ON fixing switch SW, and always turn the upper arm that is not measured.
5) Turn on the 3Φ AC input. If necessary, use a reactor or sliding voltage regulator so that the rectifier bridge will not be destroyed by the inrush surge current.
6) Apply noise with the noise simulator. Set the noise pulse width to 1 µs, set V_p to the specified value, and confirm the set value with the oscilloscope OSC_2. The fall time depends on the specified value of the noise simulator.
7) Measure the collector current i_C on the lower arm and the fault output voltage $v_{FO(N)}$ / v_{ALM} and confirm that there is no erroneous fault output or malfunction current within the specified noise applying time. In case of malfunction, over current due to short circuit through P terminal to N terminal flows and is quickly cut off by the protection function, so it is desirable to connect the snubber capacitor C_S.
8) Increase V_p as necessary and confirm the V_p at which the malfunction current or fault output occurs. When the measurement is completed, turn off all the power supplies in the reverse order of start-up.
9) Connect the output polarities of the noise simulator in reverse and perform steps d) to h). If necessary, perform steps c) to i) for other phases of the 3Φ AC input. However, it is not possible to apply noise to the ground phase.

– Specified conditions

a) Pull-up resistor R_1, R_2;

b) Voltage of control circuit power supply B_1, B_2;

c) Voltage of 3Φ AC input;

d) Voltage V_p of the noise simulator;

e) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

Bibliography

IEC 60112:2020, *Method for the determination of the proof and the comparative tracking indices of solid insulating materials*

IEC 60950-1:2005, *Information technology equipment – Safety – Part 1: General requirements*

IEC 61287-1:~~2005~~2014, *Railway applications – Power converters installed on board rolling stock – Part 1: Characteristics and test methods*

IEC 62368-1:2018, *Audio/video, information and communication technology equipment – Part 1: Safety requirements*

IEC 62477-1:2022, *Safety requirements for power electronic converter systems and equipment – Part 1: General*

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IEEJ JEC-2408:2019, *Intelligent Power Semiconductor Modules (IPM)*

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IEC 60747-15

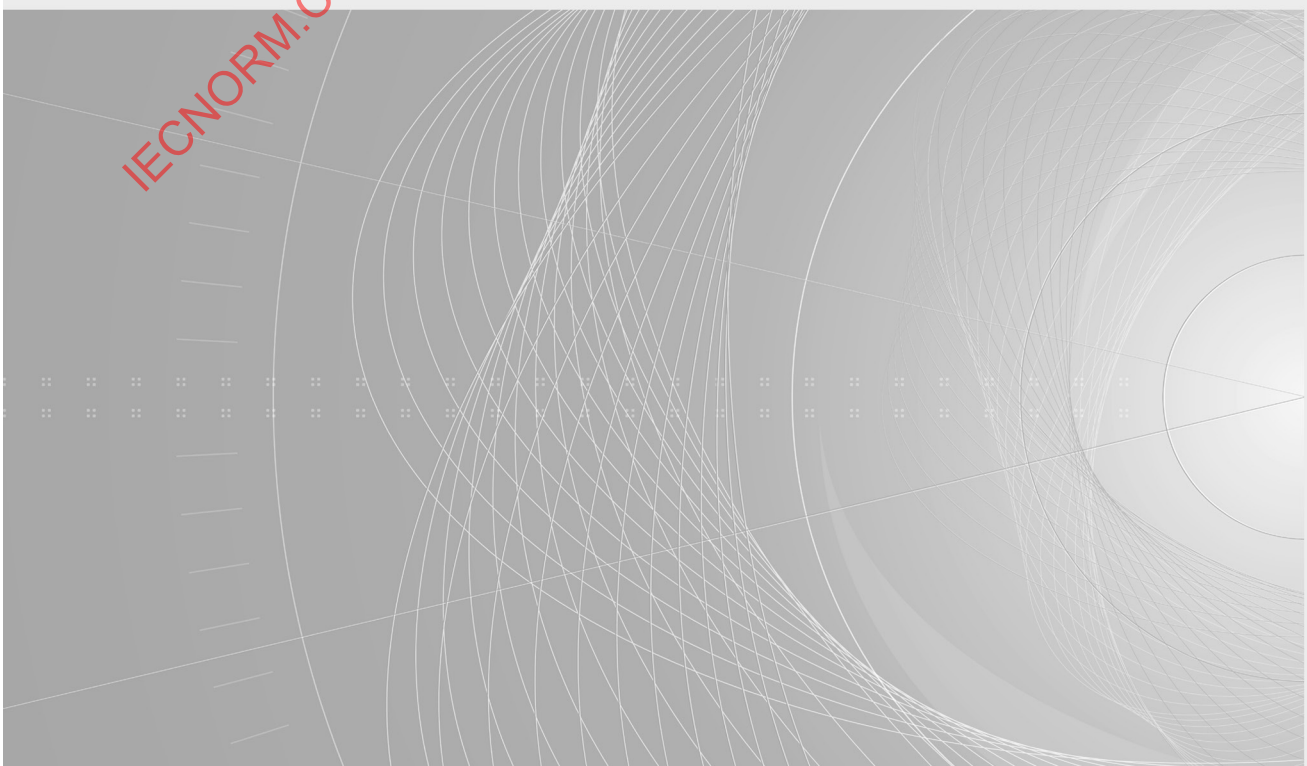
Edition 3.0 2024-10

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices –
Part 15: Discrete devices – Isolated power semiconductor devices

Dispositifs à semiconducteurs –
Partie 15: Dispositifs discrets – Dispositifs de puissance à semiconducteurs isolés



IEC 60747-15:2024-10(en-fr)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES –

Part 15: Discrete devices – Isolated power semiconductor devices

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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IEC 60747-15 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

This third edition cancels and replaces the second edition published in 2010. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) The intelligent power semiconductor modules (IPM), which was previously excluded from the first and second edition, is now included in this document (Annex C);
b) The thermal resistance is described for each switch (6.2.4);
c) Added isolation test between temperature sensor and terminals, in case there is an agreement with the user (6.1.2).

The text of this International Standard is based on the following documents:

Draft	Report on voting
47E/832/FDIS	47E/844/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

This International Standard is to be used in conjunction with IEC 60747-1:2006 and Amendment 1: 2010.

A list of all parts in the IEC 60747 series, published under the general title *Semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

SEMICONDUCTOR DEVICES –

Part 15: Discrete devices – Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the requirements for isolated power semiconductor devices. These requirements are additional to those given in other parts of IEC 60747 for the corresponding non-isolated power devices and parts of IEC 60748 for ICs.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-1:2007, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60270:2015, *High-voltage test techniques – Partial discharge measurements*

IEC 60664-1:2020, *Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests*

IEC 60721-3-3:2019, *Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*
IEC 60747-1:2006/AMD1:2010

IEC 60747-2:2016, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6:2016, *Semiconductor devices – Part 6: Thyristors*

IEC 60747-7:2019, *Semiconductor discrete devices and integrated circuits – Part 7: Bipolar transistors*

IEC 60747-8:2021, *Semiconductor devices – Part 8: Field-effect transistors*

IEC 60747-9:2019, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 60748 (all parts), *Semiconductor devices – Integrated circuits*

IEC 60749-5:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-10:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock*

IEC 60749-12:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency*

IEC 60749-15:2020, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices*

IEC 60749-21:2011, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-25:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-34:2010, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
isolated power semiconductor device
semiconductor power device that contains an integral electrical insulator between the cooling surface or base plate and any isolated circuit elements

3.2
constituent parts of the isolated power semiconductor device

3.2.1
switch
any single component that performs a switching function in an electrical circuit, e.g. diode, thyristor, MOSFET, etc.

Note 1 to entry: A switch might be a parallel or series connection of several chips with a single functionality.

3.2.2
base plate
part of the package having a cooling surface that transfers the heat from inside to outside

3.2.3
main terminal
terminal having a high potential of the power circuit and carrying the main current

Note 1 to entry: The main terminal can comprise more than one physical connector.

3.2.4
control terminal
terminal having a low current capability for the purpose of control function, to which the external control signals are applied or from which sensing parameters are taken

3.2.4.1
high voltage control terminal
terminal electrically connected to an isolated circuit element, but carrying only low current for control function

Note 1 to entry: Examples include current shunts and collector sense terminals having the high potential of the main terminals.

3.2.4.2
low voltage control terminal
terminal having a control function and isolated from the high voltage control terminals

Note 1 to entry: Examples include the terminals of isolated temperature sensors and isolated gate driver inputs, etc.

3.2.5
insulation layer
integrated part of the device case that insulates any part having high potential from the cooling surface or external heat sink and any isolated circuit element

3.3
peak case non-rupture current
peak current, which will not lead to a rupture of the package, ejecting plasma and massive particles under specified conditions

3.4
thermal interface material
heat conducting material between base plate and external heat sink

4 Letter symbols

4.1 General

General letter symbols are defined in Clause 4 of IEC 60747-1:2006.

4.2 Additional subscripts/symbols

p parasitic

t terminal

isol isolation

4.3 List of letter symbols

4.3.1 Voltages and currents

Terminal current	I_{tRMS}
Isolation voltage	V_{isol}
Partial discharge inception voltage	V_{i}
Partial discharge extinction voltage	V_{e}
Isolation leakage current	I_{isol}

4.3.2 Mechanical symbols

Mounting torque for screws to heat sink	M_s
Mounting torque for terminal screws	M_t
Mounting force	F
Acceleration in all 3 axis (x, y, z)	a
Mass	m
Flatness of the case (base plate)	e_c
Flatness of the heat sink surface	e_s
Roughness of the case (base plate)	R_{Zc}
Roughness of the heat sink surface	R_{Zs}
Thickness of thermal interface material (case – heat sink)	$d_{(c\text{-}s)}$

4.3.3 Other symbols

Parasitic inductance, effective between terminals and chips	L_p
Parasitic capacitance between terminals and cooling surface (case, base plate, ground)	C_p
Lead resistance between terminal x and internal device connection x'	r_{xx}
Terminal temperature	T_t
Number of power load cycles until failure of a percentage p of a population of devices	$N_{f;p}$

5 Essential ratings (limiting values) and characteristics

5.1 General

Isolated power semiconductor devices should be specified as case rated or heat sink rated devices. The ratings and characteristics should be quoted at a temperature of 25 °C or another specified elevated temperature. Requirements for multiple devices having a common encapsulation are described in 5.12 of IEC 60747-1:2006.

5.2 Ratings (limiting values)

5.2.1 Isolation voltage or isolation test voltage (V_{isol})

Maximum RMS or DC value between main terminals and high voltage control terminals at one side and low voltage control terminals (where appropriate) and base plate at the other side for a specified time.

5.2.2 Peak case non-rupture current (where appropriate)

Maximum value for each main terminal that does not cause the bursting of the case or emission of plasma and particles.

5.2.3 Terminal current (I_{tRMS}) (where appropriate)

Maximum RMS value of the current through the main terminal under specified conditions at minimum mounting torque M_t and maximum allowed terminal temperature (T_{tmax} = T_{stg} or T_{tmax} ≤ T_{vjmax}).

5.2.4 Temperatures

5.2.4.1 Solder temperature (T_{sold}) (where appropriate)

Maximum solder temperature T_{sold} during solder process over a specified solder processing time t_{sold}.

5.2.4.2 Storage temperature (T_{stg})

Minimum and maximum storage temperature.

5.2.5 Mechanical ratings

5.2.5.1 Mounting torque for screws to heat sink (M_s)

Minimum and maximum mounting torque that shall be applied to the fixing screws to the heat sink.

5.2.5.2 Mounting torque for screws to terminals (M_t)

Minimum and maximum mounting torque that shall be applied to screwed terminals.

5.2.5.3 Mounting force (F)

Minimum and maximum mounting force for pressure mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device.

5.2.5.4 Terminal pull-out force (F_t)

Maximum force.

5.2.5.5 Acceleration (a)

Maximum value along each axis (x, y, z).

5.2.5.6 Flatness of the heat sink surface (e_s) (where appropriate)

Maximum deviation from flatness for the heat sink surface over the whole mounting area.

5.2.5.7 Roughness of the heat sink surface (R_{Zs}) (where appropriate)

Maximum roughness of the heat sink surface over the whole mounting area.

5.2.6 Climatic ratings (where appropriate)

Limiting values of environmental parameters for the final application as follows:

– ambient temperature;
– humidity;
– speed and pressure of air;
– irradiation by sun and other heat sources;
– mechanical active substances;
– chemically active substances;
– biological issues,

shall be described in classes as specified in IEC 60721-3-3:2019, Table 1.

5.3 Characteristics

5.3.1 Mechanical characteristics

5.3.1.1 Creepage distance along surface (d_s)

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate.

NOTE 1 IEC 60112:2020 (details to comparative tracking index "CTI") and IEC 60664-1:2020, 5.2 apply.

NOTE 2 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance considerably (details see 60664-1:2020, examples). This is essential, if dust, moisture or dirt starts to cover the surface and increases the leakage current over surface, which might start burning the plastic encapsulation material.

5.3.1.2 Clearance distance in air (d_a)

Minimum value of distance through air between terminals of different potential of the isolated device and to base plate.

NOTE For details, see IEC 60664-1:2020, 4.6 and 5.1 which show typical examples of various shapes of clearance distances.

5.3.1.3 Mass (m) of the device

Maximum value excluding accessories (mounting hardware).

5.3.1.4 Flatness of the case (base plate) (e_c) (where appropriate)

Maximum and minimum allowed deviation from flatness for the base plate and its direction (convex or concave).

5.3.2 Parasitic inductance (L_p)

Maximum or typical value between the main terminals of each main current path.

5.3.3 Parasitic capacitances (C_p)

Maximum value of parasitic capacitance between the specified main terminal(s) and the cooling surface.

5.3.4 Partial discharge inception voltage (V_{iM} or $V_{i(RMS)}$) (where appropriate)

Minimum peak value V_{iM} or RMS value $V_{i(RMS)}$ between the isolated terminals and the base plate (details, see IEC 60270:2015).

5.3.5 Partial discharge extinction voltage (V_{eM} or $V_{e(RMS)}$) (where appropriate)

Minimum peak value V_{eM} or RMS value $V_{e(RMS)}$ between the isolated terminals and the base plate (for details, see IEC 60270:2015).

5.3.6 Thermal resistances

5.3.6.1 Thermal resistance junction to case for case rated devices ($R_{th(j-c)X}$)

Maximum value of thermal resistance junction to a specified reference point at the case (base plate) per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)).

5.3.6.2 Thermal resistance case to heat sink ($R_{th(c-s)}$) (where appropriate)

Maximum or typical value of thermal resistance between two specified points at the case and at the heat sink of the case rated device ("module"), when the case is mounted according to manufacturer's mounting instructions.

5.3.6.3 Thermal resistance case to heat sink per switch ($R_{th(c-s)X}$) (where appropriate)

Maximum or typical value of thermal resistance between the two specified points of the case and the heat sink of the switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)) of the isolated case rated devices ("module"), when the case is mounted according to the manufacturer's mounting instructions.

5.3.6.4 Thermal resistance junction to heat sink for heat sink rated devices ($R_{th(j-s)X}$)

Maximum or typical value of thermal resistance junction to a specified point at the heat sink per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)), when the device is mounted according to the manufacturer's mounting instructions.

5.3.6.5 Thermal resistance junction to sensor ($R_{th(j-r)}$) (where appropriate)

Value of thermal resistance junction to an integrated temperature sensor when the device is mounted according to the manufacturer's mounting instructions.

The position of this thermal resistance should be shown in the thermal resistance equivalent circuit.

5.3.7 Transient thermal impedance (Z_{th})

Thermal impedance as a function of the time elapsed after a step change of power dissipation for each thermal resistance specified in 5.3.6 and shall be specified in one of the following ways.

6 Measurement methods

6.1 Verification of isolation voltage rating

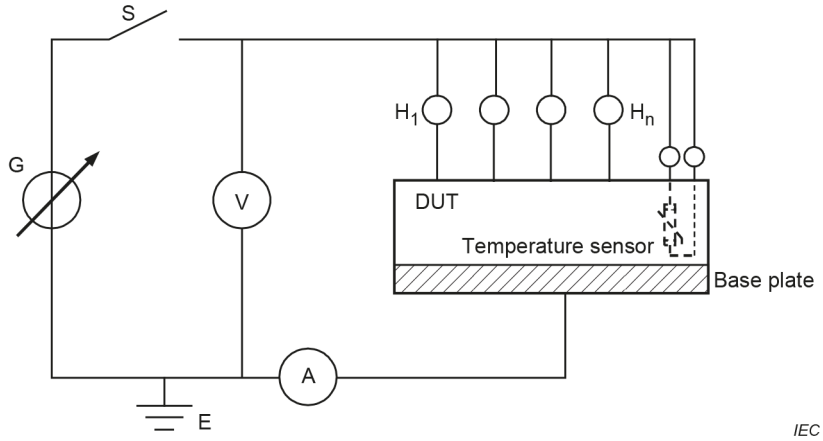
6.1.1 Verification of isolation voltage rating between terminals and base plate (V_{isol})

– Purpose

  Proof of the ability of the isolated power device to withstand the rated isolation voltage.

– Circuit diagram

  See Figure 1.



Key

DUT	device under test
G	voltage source with high impedance, capable to supply V_{isol}
S	main switch
V	voltmeter for V_{isol}
A	ammeter or current probe for Iisol
$H_1 \ldots H_n$	high potential terminal

Figure 1 – Basic circuit diagram for isolation breakdown withstand voltage test ("high pot test") with V_{isol}

The voltage source G is capable to supply the isolation voltage V_{isol} as the AC or DC voltage with a high internal impedance to limit the possible breakthrough current in case of breakdown of the DUT.

All main terminals and high voltage control terminals are connected together and connected to the high potential output terminal H of the voltage source G. The base plate of the DUT, respectively its metallized cooling surface and all low voltage terminals are connected to ground potential E. An amperemeter or current probe A is applied to measure the isolation leakage current.

If there is an agreement with user, perform an isolation test between the temperature sensor and the terminals (V_{isol1}) (See 6.1.2).

– Test procedure

Switch S is closed and the voltage is slowly raised to the specified value and maintained at that value for the specified time. The current measured on ammeter A shall not exceed the specified value. The voltage is then reduced to zero.

– Specified conditions

Specified in IEC 60664-1:2020.

- Ambient or case temperature
- V_{isol}
- I_{isol} as maximum test limit
- Test time t, if less than 60 s.

6.1.2 Verification of isolation voltage rating between temperature sensor and terminals (V_{isol1})

– Purpose

To verify that the isolation voltage between the temperature sensor and the other terminals in case the temperature sensor is connected to the base plate potential.

– Circuit diagram

See Figure 2.

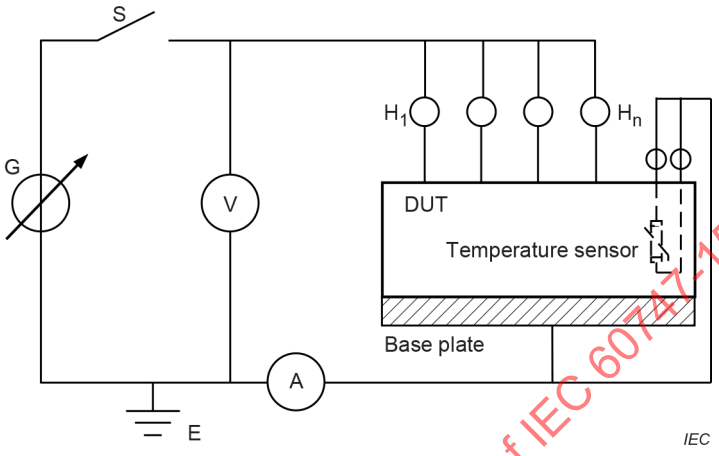


Figure 2 – Basic circuit diagram for isolation voltage test between temperature sensor and terminals (V_{isol1})

– Circuit description and requirements, test procedure and specified conditions

Similar as described in 6.1.1, but optionally a lower test voltage V_{isol1} may be specified and applied.

6.2 Methods of measurement

6.2.1 Partial discharge inception and extinction voltages (V_i) (V_e)

Between high potential terminals and base plate (where appropriate). See IEC 60270:2015 and IEC 60664-1:2020.

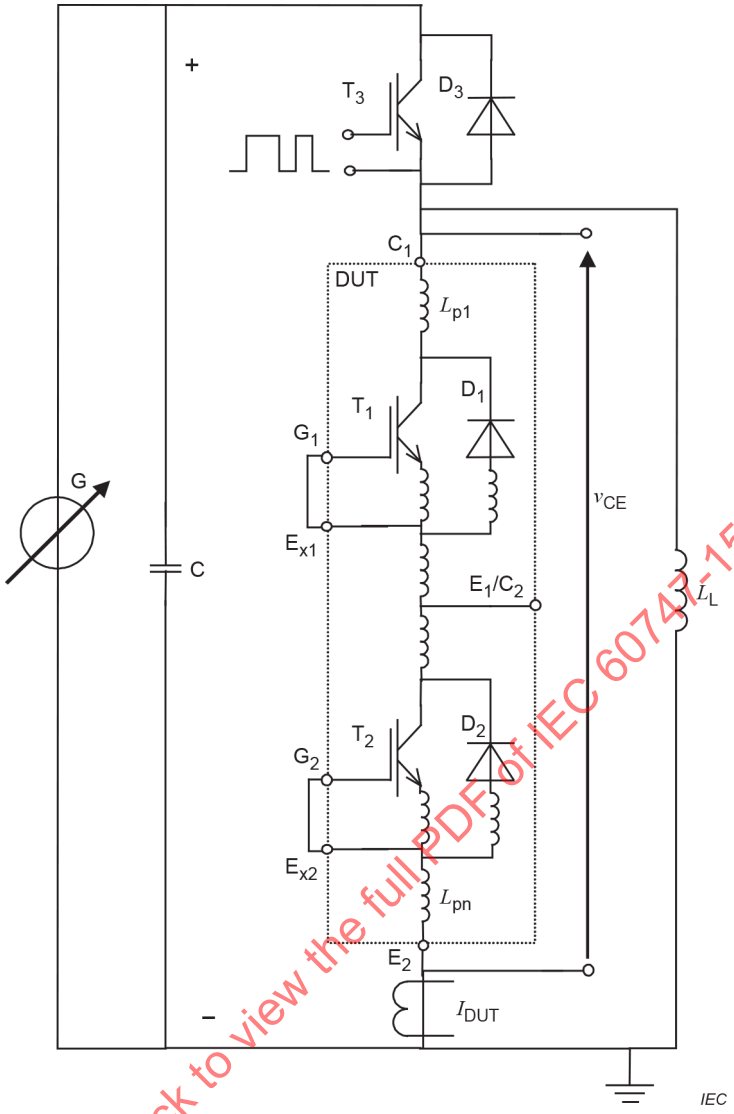
6.2.2 Parasitic inductance (L_p)

– Purpose

To measure the parasitic inductance between two main terminals.

– Circuit diagram

See Figure 3.



Key

DUT	device under test T_1+T_2, for example IGBT (Single or Dual – shown – or branch of a three phase arrangement), fast diode or MOSFET device
C	main capacitor bank as reservoir
L_L	load inductance, at least 100 times the parasitic inductance
L_{p1} ...L_{pn}	portions of parasitic inductance L_p
I_{DUT}	current probe
G	voltage source to charge the capacitor
T_1	DUT, top switch (shown as IGBT in Figure 3)
T_2	DUT, bottom switch (shown as IGBT in Figure 3), optional
T_3	auxiliary IGBT switch

Figure 3 – Circuit diagram for measurement of parasitic inductances (L_p)

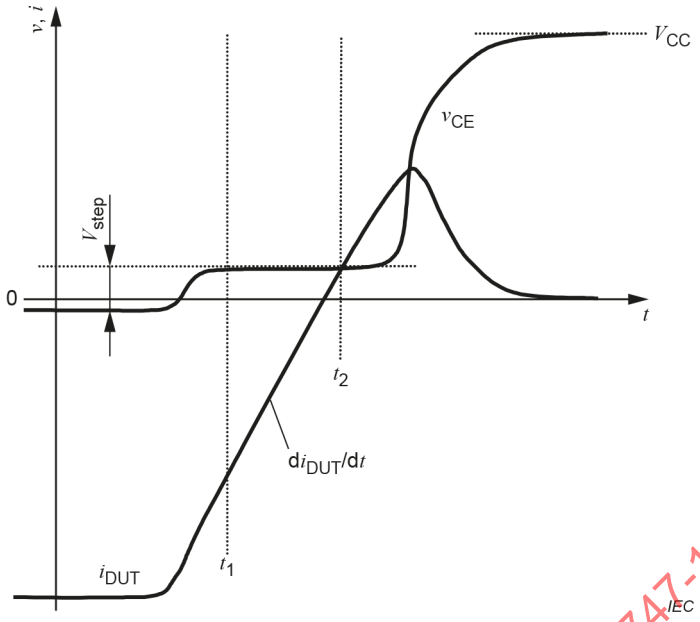


Figure 4 – Wave forms

– Circuit description and requirements

The circuit of Figure 3 consists of a DC supply G for the charge reservoir C; T_3 is an auxiliary switch, a gate drive unit for T_3, the DUT inserted into the test set-up with the gate control terminals shorted, a dual channel oscilloscope, which senses the voltage v_{CE} between main terminals "C_1" and "E_2", a current probe, which senses the current i_{DUT} through the diode path of the DUT, connected to the dual channel oscilloscope. This measuring method uses reduced voltage V_{CC} and the di/dt of diodes incorporated in the device at switch-off, sensing the voltage at outside main terminals. This is usable for single switch devices as well as for half bridge circuit devices (DUAL modules).

– Measurement procedure

The waveforms observed by this measurement shown in Figure 4.

A pulsed current method is used. Auxiliary transistor T_3 switches the load current to the inductor L_L on and off. When T_3 is off, the current freewheels via the diodes of the DUT. When T_3 switches on again, it causes the current through the diodes to fall at an almost linear rate di_{DUT}/dt. During this time (t_1 –t_2), the voltage across the DUT forms at step of V_{step} caused by the internal parasitic inductance at current decline (di_{DUT}/dt). The value of the parasitic inductance of the main current path can be calculated from

$$L_p = V_{step} / |(di_{DUT}/dt)| \quad (1)$$

Use low inductance (sheeted) bus baring and low inductance current probe.

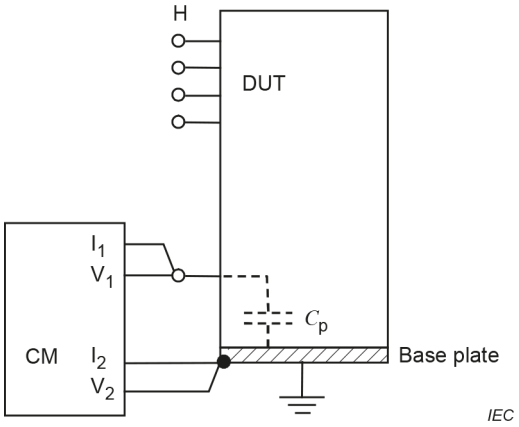
6.2.3 Parasitic capacitance terminal to case (C_p)

– Purpose

To measure the parasitic capacitance C_p between specified main terminal(s) and the case (base plate)

– Circuit diagram

See Figure 5.



Key

C_p	parasitic capacitance
H	high potential terminal
CM	capacitance meter

Figure 5 – Circuit diagram for measurement of parasitic capacitance (C_p)

– Measurement procedure

Mount the device to a grounded heat sink according to the manufacturer's mounting instructions. Connect the current source connector "I_1" of the capacitance meter CM to the specified terminal and connector "I_2" to ground (base plate) of the DUT. Connect the voltage sensing connector of the capacitance meter to test points "V_1" and "V_2" to ground. CM is set to the specified frequency. The capacitance C_p can be read on CM. For the measurement of the total coupling capacitance C_p connect all main terminals to each other and proceed with the measurement as described above.

– Specified conditions

- Measurement frequency f of the CM.

6.2.4 Thermal characteristics

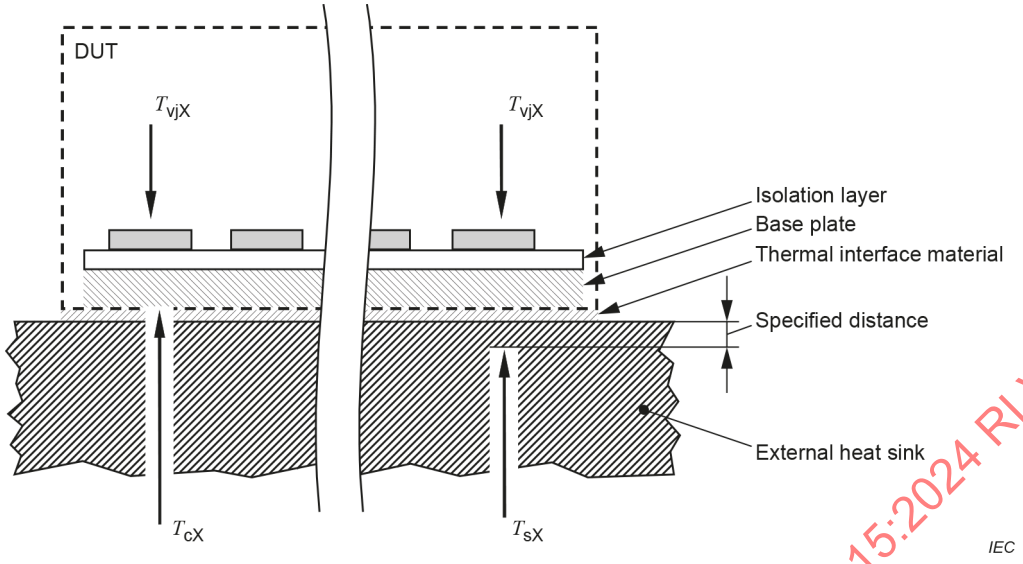
6.2.4.1 General description of measuring methods

– Purpose

To measure thermal characteristics between the switch and the cooling system.

– Reference points for temperature measurement and description

Same methods should be used as for the corresponding non-isolated device. Thermal resistance and impedance are measured in the same way as described in the documents for diodes IEC 60747-2:2016, thyristors IEC 60747-6:2016, bipolar transistors IEC 60747-7:2019, FETs IEC 60747-8:2021 and IGBTs IEC 60747-9:2019.



Key

T_{vjX} junction temperature of chip X

T_{cX} case temperature under chip X

T_{sX} heat sink temperature under chip X

Figure 6 – Cross-section of an isolated power device with reference points for temperature measurement of T_c and T_s

– Measurement procedure

Cross-sectional view of an isolated power device is shown in Figure 6.

T_{cX} is measured by a temperature measuring instrument from underneath through a small hole through the heat sink and any thermal interface material underneath the switch X(chip). T_{sX} is taken from above at hottest accessible point, nearest to the switch X(chip) or from underneath through a specified sack hole ending at 2 (±1) mm below the heat sink surface (to be specified, type test feature). T_{vjX} is determined using indirect methods like described in the individual documents.

The thermal resistance $R_{th(j-s)}$ and $R_{th(c-s)}$ depends on several mechanical parameters such as type and thickness of the used thermal interface material (should be specified in manufacturer's mounting instructions, for example 30 to 50∝m), the maximum deviation of flatness of the cooling surface of the device's base plate and of the heat sink and the mounting torque of the fixing screws, as per specified mounting instructions.

6.2.4.2 Thermal resistance junction to case per switch (X) $R_{th(j-c)X}$

$$R_{th(j-c)X} = (T_{vjX} - T_{cX})/P_X \quad (2)$$

where

X is the D (Diode), T(Thyristor), I (IGBT), M (MOSFET), B(BJT);

T_{vjX} is the virtual junction temperature of the switch X;

T_{cX} is the temperature of the case (base plate) under the switch X(chip);

P_X is the applied power dissipation at the each switch D,T,I,M,B.

Second index might be needed to distinguish multiple devices in one product (e.g., Inverter IGBTs and Brake IGBTs).

6.2.4.3 Thermal resistance case to heat sink per switch (X) $R_{th(c\text{-}s)X}$ or per device $R_{th(c\text{-}s)}$

$$R_{th(c\text{-}s)X} = (T_{cX} - T_{sX})/P_X \quad (3)$$

where

X is the D (Diode), T(Thyristor), I (IGBT), M (MOSFET), B(BJT);

T_{cX} is the temperature taken at the specified point of the case (as above) under the chip;

T_{sX} is the temperature of the heat sink, taken at the reference point for testing T_s specified;

P_X is the applied power dissipation at the each switch D,T,I,M,B;

P is the whole applied power dissipation of the device.

Second index might be needed to distinguish multiple devices in one product (e.g., Inverter IGBTs and Brake IGBTs).

– Specified conditions
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

NOTE See Annex B for measuring method of the thickness of thermal interface material.

6.2.4.4 Thermal resistance junction to heat sink per switch (X) $R_{th(j\text{-}s)X}$ (for heat sink rated devices)

$$R_{th(j\text{-}s)X} = (T_{vjX} - T_{sX})/P_X \quad (4)$$

where

X is the D (Diode), T(Thyristor), I (IGBT), M (MOSFET), B(BJT);

T_{vjX} is the virtual junction temperature of the switch X;

T_{sX} is the temperature of the heat sink, taken at the reference point for testing T_s specified;

P_X is the applied power dissipation at the each switch D,T,I,M,B.

Second index might be needed to distinguish multiple devices in one product (e.g. Inverter IGBTs and Brake IGBTs).

– Specified conditions
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement

6.2.4.5 Transient thermal impedance Z_{th}

– Measurement circuit and procedure

These are based on 6.2.4.2 to 6.2.4.4. Individual documents of the non-insulated devices apply.

$$Z_{th(j\text{-}c)X} = (|T_{vjX}(0) - T_{cX}(0)| - |T_{vjX}(t) - T_{cX}(t)|) / P_X \quad (5)$$

$$Z_{th(c\text{-}s)X} = (|T_{cX}(0) - T_{sX}(0)| - |T_{cX}(t) - T_{sX}(t)|) / P_X \quad (6)$$

$$Z_{th(j\text{-}s)X} = (|T_{vjX}(0) - T_{sX}(0)| - |T_{vjX}(t) - T_{sX}(t)|) / P_X \quad (7)$$

– Specified conditions
  - Mounting according manufacturer's instructions
  - Thermal conductivity of the thermal interface material
  - Reference points for thermal measurement.

7 Acceptance and reliability

7.1 General requirements

In addition to the following subclauses, the requirements applicable to the non-isolated devices as given in the other relevant parts of IEC 60747 apply.

7.2 List of endurance tests

See Table 1.

Table 1 – Endurance tests

Subclause	Environmental testing – designation	Short form	Normative reference
7.2.1	High temperature reverse bias or high temperature blocking	HTRB	IEC 60749-5
7.2.2	High humidity and high temperature reverse bias or high humidity and high temperature blocking	H^3TRB	IEC 60749-5
7.2.3	Power cycling (load) capability		IEC 60749-34
7.2.4	High temperature storage	HTS	IEC 60749-6
7.2.5	Low temperature storage	LTS	IEC 60068-2-1
7.2.6	Thermal cycling	TC	IEC 60749-25
7.2.7	Resistance to solder heat		IEC 60749-15
7.2.8	Solderability		IEC 60749-21
7.2.9	Mechanical shock		IEC 60749-10
7.2.10	Vibration (variable frequency)		IEC 60749-12

7.3 Acceptance defining criteria

See Table 2.

Table 2 – Acceptance defining characteristics for endurance and reliability tests

Acceptance defining characteristic	Acceptance criteria	Measurement conditions
I_{isol}	< USL	Specified V_{isol}
R_{th}	< USL	Mounting instructions
USL: upper specification limit.		

7.4 Type tests and routine tests

7.4.1 Type tests

The experience which has been obtained with other isolated power semiconductor devices, using the same or similar components such as switches or packages, should be considered when deciding which tests are mandatory.

Type tests are carried out on new products on a sample basis, in order to determine the electrical and thermal and mechanical and climatic ratings (limiting values) characteristics to be given in the data sheet and to establish the test limits for future routine tests. Some or all of the tests should be repeated from time to time on samples drawn from current production or deliveries so as to confirm that the quality of the product continuously meets the requirements.

The minimum type tests to be carried out are as follows.

New isolated power semiconductor devices should undergo the type tests listed in Table 3, marked with "X" (X = mandatory). Some of the type tests are destructive.

Table 3 – Minimum type and routine tests for isolated power semiconductor devices

Subclause	Items	Type test	Routine test	Destructive
5.2.1, 6.1	Isolation voltage (V_{isol}), (V_{isol1})	X	X	
5.2.2, Annex A	Peak case non-rupture current	X[a]		X
5.3.1	outline dimensions, creepage, clearance	X		
5.3.1.4	flatness of base plate	X	X[b]	
5.3.6, 6.2.4	thermal resistances (R_{th})	X		
5.3.7, 6.2.4.5	transient thermal impedance (Z_{th})	X		
5.3.2, 6.2.2	parasitic inductance (L_p)	X[a]		
5.3.3, 6.2.3	parasitic capacitance (C_p)	X[a]		
5.3.4, 5.3.5, 6.2.1	partial discharge voltages (V_{iM} or $V_{i(RMS)}$) / (V_{eM} or $V_{e(RMS)}$)	X[a]	X[b]	
5.2.5.4	terminal pull-out force (F_t)	X		X
7.2.6[c]	thermal cycling	X		X
7.2.3[c]	power cycling (load)	X		X
7.2.9 [c],7.2.10[c]	mechanical shock, vibration	X		X
5.2.6	climatic ratings	X[a]		

NOTE Tests for isolation voltage, partial discharge voltage, creepage and clearance distance should be based on each standard which should be applied to any final equipment using the isolated power semiconductor device. For example, see IEC 62368-1, IEC 61287-1, etc.

[a] Type test only for devices with specified maximum values.

[b] Routine test only for devices with specified maximum or minimum values.

[c] See Table 1 for normative references of test·

7.4.2 Routine tests

The routine tests should be carried out on the current production or deliveries normally on a 100 % basis. The ratings and characteristics specified in the data sheet should be verified for each criterion or specimen. Routine test may comprise a selection of the isolated devices into groups of routine tests in Table 3. The minimum routine tests to be carried out on isolated devices are listed in Table 3. Other routine tests are carried out as described in the other parts of the IEC 60747, which is valid for the particular switch.

Annex A
(informative)

Test method of peak case non-rupture current[1]

A.1 Purpose

To prove the ability of the isolated power device containing bipolar transistors, IGBTs or MOSFETs as switches to withstand the rated peak case non-rupture current without causing a rupture (an "explosion") of the case or an emission of plasma beam or ejecting massive particles. This is a destructive test.

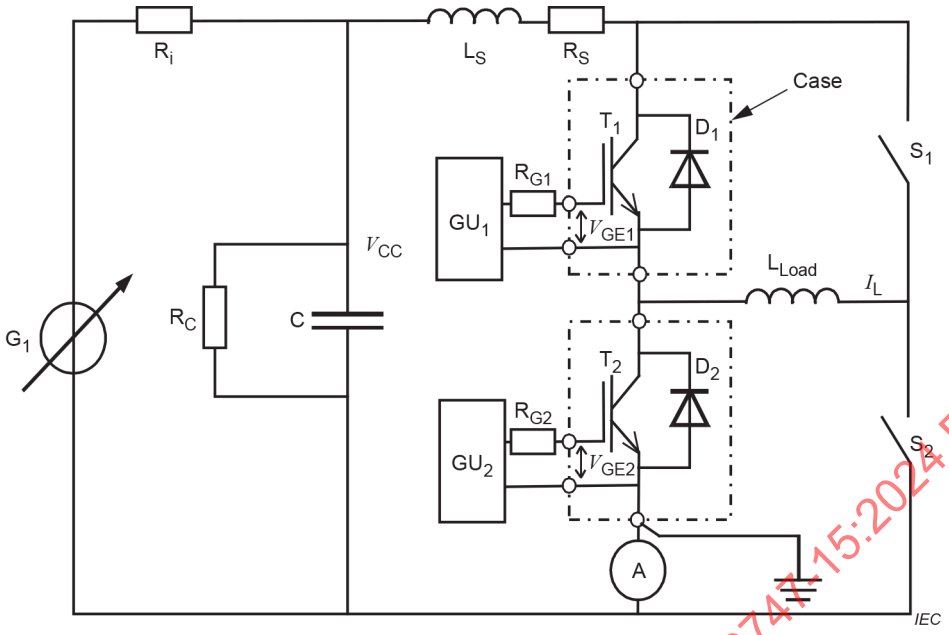
Case rupture is caused by inside arc or vapour pressure, when the supplied energy or current from outer source exceeds the specified limit. The arc or vapour pressure is induced in a package (encapsulation) of failed power devices by being supplied with stored energy or current from an outer circuit power source. Critical current or energy for packages after the device failure should be issued as an item of the package environmental properties, and in addition the semiconductor and also other electrical parts should avoid an explosion by accident.

NOTE Annex A is applicable if there is an agreement with user.

A.2 Circuit diagram

See Figure A.1.

1 Still under discussion.



Key

A	Ammeter to measure the device current which can be peak case non-rupture current, if the case did not burst, monitored by a current probe having low inductance
C	line capacitor bank, chargeable to full voltage
D_1	inverse diode of T_1, high side
D_2	inverse diode of T_2, low side
G_1	DC supply voltage source V_{CC}, which can be switched off from mains under all conditions
GU_1	gate drive unit of T_1
GU_2	gate drive unit of T_2
L_{Load}	load inductance
L_s	stray inductance of the circuit (specified value)
R_c	discharge resistor for protection purposes
R_{G1}	gate resistor of T_1
R_{G2}	gate resistor of T_2
R_i	internal source resistance
R_s	fuse resistor, mostly set to zero
S_1	auxiliary switch (IGBT), high side
S_2	auxiliary switch (IGBT), low side
T_1	high side IGBT switch = device under test (DUT)
T_2	low side IGBT switch
I_L	load current
V_{GE1}	gate voltage of T_1
V_{GE2}	gate voltage of T_2

Figure A.1 – Circuit diagram for test of peak case non-rupture current

The set-up consists of a two-quadrant converter with two identical isolated IGBT devices. S_1 and S_2 are auxiliary switches, for example IGBT devices, used to establish the desired load current and to induce a short circuit failure. T_1 and T_2 are identical isolated IGBT devices (SINGLE switch or both in a half bridge circuit as DUAL switch). This Annex A describes testing methods using S2.

A.3 Test procedure

- Test A:

  First, close switch S_2, turn on T_1, the load current increases as defined by load inductance L_{Load}. After I_L have exceeded the safe operating area (SOA) for turn-off of T_1, it is attempted to turn off T_1. The initial part of the turn-off process takes place, the current in the device is reduced and part of the current is commuted to the diode D_2. The device T_1 then undergoes a turn-off failure. The diode in the low side device D_2 carries substantial current at this instant. The failure of T_1 forces the diode D_2 to turn off at virtually unlimited di/dt, drawn by L_{Load}. This is outside the diode SOA, and the diode D_2 also fails.

- Test B:

  T_1 is turned on until a substantial load current is reached. At this moment the device T_2 is turned on. It is induced to fail, because it sees the full voltage together with full current. The device T_1 then goes into desaturation and also fails.

These tests are executed until a value of stored energy of the capacitor bank and of peak current is found, which is not high enough to rupture or break the case. The values of achieved peak current I_C = peak case non-rupture current, V_{CC}, C_{max} and of $E_C = ½ CV_{CC}^2$ are monitored.

A.4 Post test measurements and criteria

The DUT is subjected to a visual test, whether cracks and signs of plasma from arcing inside are visible from outside. There shall be no signs of particles thrown out nor shall there be evidence that the device has externally melted or burst into flames.

A.5 Specified conditions

- Case or virtual junction temperature (T_c = 25 °C, T_{vj} = 25 °C or 125 °C)
- Supply voltage V_{CC}
- Capacitance of capacitor bank C
- Stored energy of capacitor bank E_C
- Stray inductance of short circuit L_{SC}
- Load current I_L
- Gate voltage V_{GEon} and V_{GEoff}
- Gate resistance R_{Gon} and R_{Goff}
- Percentage of tested devices not burst to total number of tested devices.

NOTE See Bibliography.

Annex B
(informative)

Measuring method of the thickness of thermal compound paste

B.1 General

The measuring gauge is a comb out of stainless steel or suitable plastic, which is not solvable by the fluid material of the thickness of layer to be tested. The outer teeth of the comb – those at the edges of the hexagon in Figure B.1 – form a base line. The inner teeth – those between the outer teeth – are progressively shortened, so that a space of distances is achieved between the teeth and the base line. The size of the distance can be read on a scale on the instrument. A typical measuring gauge is shown in Figure B.1.

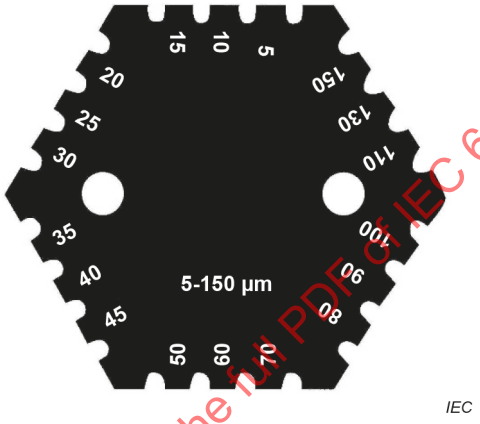


Figure B.1 – Example of a measuring gauge for a layer of thermal compound paste of a thickness between 5 µm and 150 µm

B.2 Measuring method

Immediately after applying the layer, the measuring comb is pressed upon the substrate, so that the teeth are vertical to the surface and the measuring comb does not slip. Remove the comb and look at the teeth to ensure that is the shortest tooth that still touched the fluid layer. The thickness of the layer corresponds to the average mean value of the last touching tooth and the first non-touching tooth. At least two further measurements at different parts on the surface are to be executed in same way to get representative values for the covered area.

This method measures the thickness after grease printing. Therefore, it is very effective for the start-up inspection of the printing type grease application device. However, it is not suitable for inspection of dispenser type grease application equipment or each products warranty, so it is necessary to consider another method for those verifications.

Annex C
(informative)

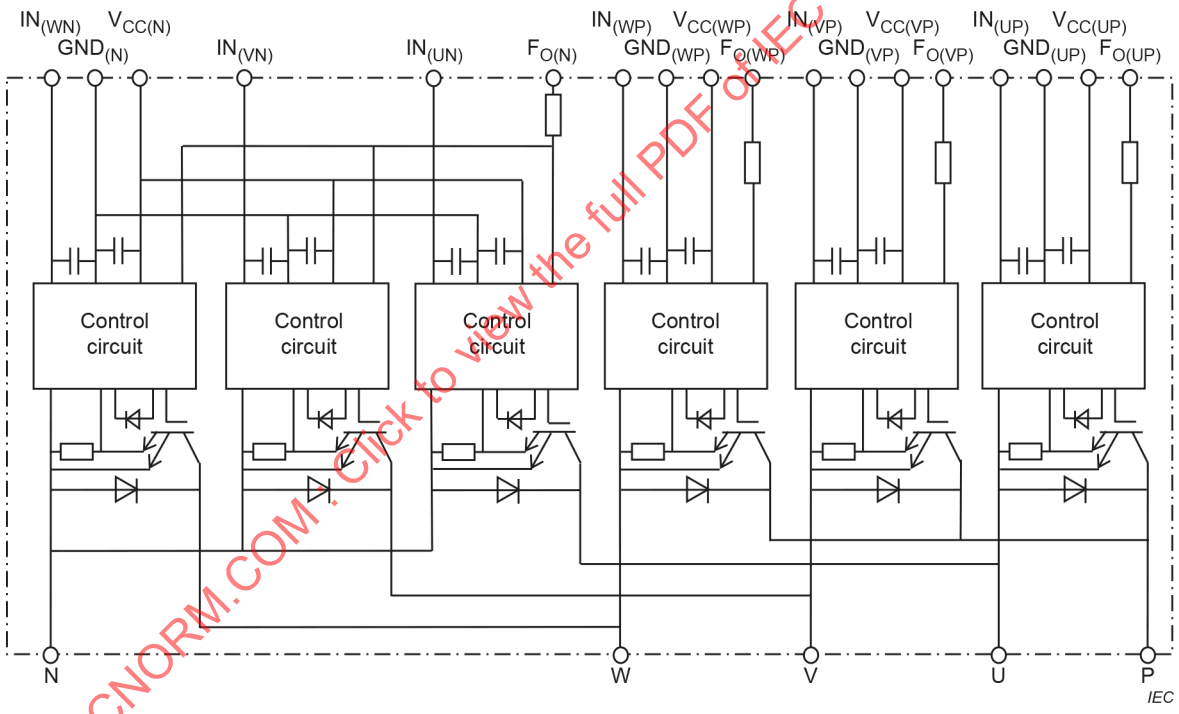
Intelligent power semiconductor modules (IPMs)

C.1 General

Isolated power semiconductor devices are categorized to several type, intelligent power semiconductor module is one of type of them. The intelligent power semiconductor modules (IPMs) include incorporated control circuits, such as gate driving circuit, protection function circuits from abnormal operation. This type of device is widely used in field, this annex shows functions of the IPM as of reference. And IGBT-IPM is used as an example in this annex. Add the descriptions for another type of IPMs if needed in the future.

C.2 Control terminals of IPM

Figure C.1 shows the internal circuit configuration block diagram of representative IPM, main terminals and control terminals.



Key

P	+DC main terminal
N	-DC main terminal
U, V, W	Output main terminals
$V_{CC(UP,VP,WP,N)}$	power supply (+) terminals for control circuits
$GND_{(UP,VP,WP,N)}$	power supply (-) terminals for control circuits / reference potential terminals
$IN_{(UP, VP, WP, UN, VN, WN)}$	input signal terminals of control circuit
$F_{O(UP, VP, WP, N)}$	alarm output terminals of control circuit

Figure C.1 – Example of internal circuit configuration block diagram of IPM

C.3 Essential ratings (limiting value) and characteristics

C.3.1 General

The ratings and characteristics of IPM regarding incorporated control circuit are described in this clause. The input signal for driving the IGBT is low active, that is, the IPM in which the IGBT is turned on when the signal level changes from High to Low is taken as an example. Figure C.1 shows an example of 6 in 1 type IPM that is widely used in the market, but from this section onwards using 2 in 1 type IPM for simplification explain.

NOTE If more than one rating or characteristic names, letter symbols are used in actual application, those are indicated by using "/" as separator.

C.3.2 Ratings (limiting value) and testing method

C.3.2.1 Supply voltage V_D / V_{CC}

Maximum voltage that can be applied between V_{CC} terminal and GND terminal under specified conditions. Both letter symbols V_D and V_{CC} may be used.

C.3.2.2 Input voltage V_{CIN} / Input signal voltage V_{in}

Maximum voltage that can be applied between IN terminal and GND terminal under specified conditions.

C.3.2.3 Fault output voltage V_{FO} / Alarm signal voltage V_{ALM}

Maximum voltage that can be applied between F_O terminal and GND terminal under specified conditions.

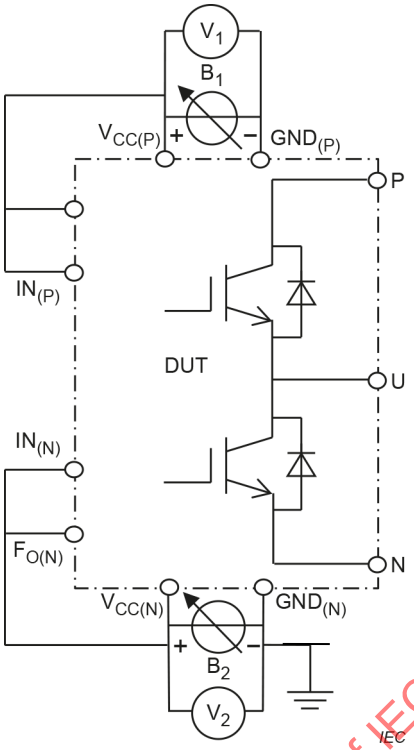
Testing method for the above three ratings is shown below.

– Purpose

  To confirm that there is no abnormality when the rated voltage of the control circuit is applied to the control circuit of the DUT under the specified conditions.

– Test circuit

  Testing circuit is shown in Figure C.2, as an example of 2 in1 type IPM.



Key

DUT IPM under test

B_1 Power supply voltage source of upper arm control circuit

B_2 Power supply voltage source of lower arm control circuit

V_1 Voltmeter for upper arm control circuit power supply observation

V_2 Voltmeter for lower arm control circuit power supply observation

Figure C.2 – Testing circuit for supply voltage, input voltage / input signal voltage, and fault output voltage / alarm signal voltage

– Test procedure

1) Connect the test circuit shown in Figure C.2 to the DUT.
2) Set the DUT to the specified temperature by a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_1, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_2.
4) Confirm that there are no abnormalities after the test.

– Specified conditions

a) Voltage of control circuit power supply B_1, B_2.
b) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.2.4 Fault output current I_{FO} / Alarm signal current I_{ALM}

Maximum current that can be flown between F_O terminal and GND terminal under specified conditions.

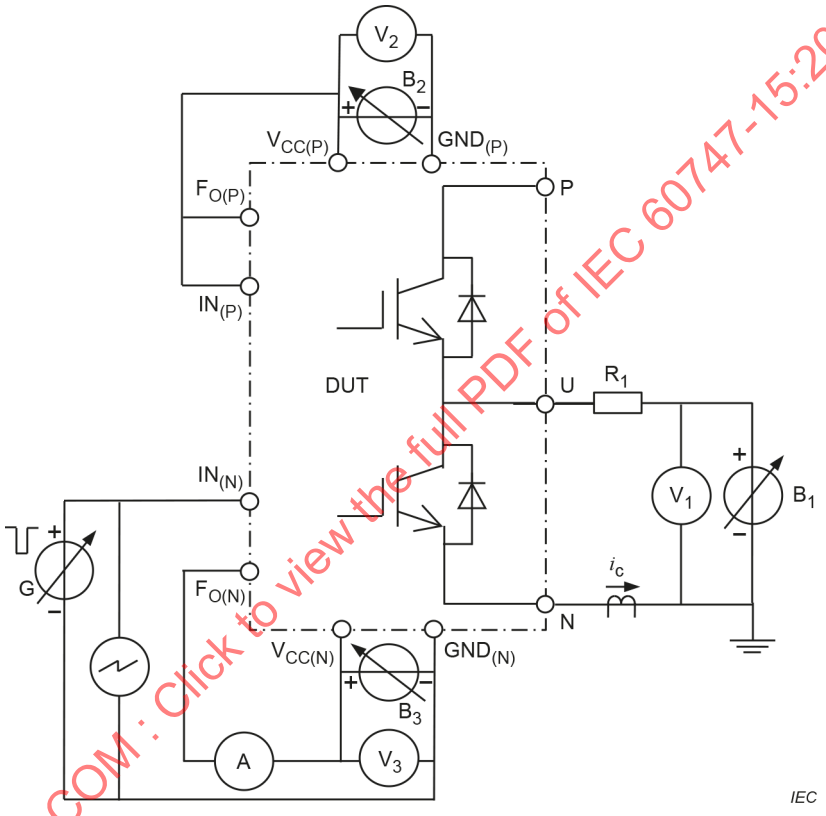
Testing method is shown below.

– Purpose

To confirm that there is no abnormality when the rated current of the control circuit is applied to the DUT control circuit under the specified conditions.

– Test circuit

Testing circuit is shown in Figure C.3.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for collector current power supply observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
OSC	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation
R_1	Current limiting resistor
A	Ammeter for fault output current observation

Figure C.3 – Testing circuit for fault output current / alarm signal current

– Test procedure

1) Connect the test circuit shown in Figure C.3 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the ON-signal between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by the Variable pulse voltage source G.
5) Increase the voltage of the power supply voltage source B_1 until over current protection / short circuit protection function is activated.
6) When the over current protection / short circuit protection is activated, observe the current flowing to the $F_{O(N)}$ terminal with an ammeter (or current sensor with oscilloscope) and confirm that it can withstand the rated current.
7) Confirm that there are no abnormalities after the test.

– Specified conditions

a) Collector current of over current protection / short circuit trip level;
b) Specified current I_{FO} or I_{ALM} to $F_{O(N)}$ terminal (adjustable by B_3 voltage);
c) Voltage of control circuit power supply B_2, B_3;
d) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
e) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.2.5 Main circuit DC bus voltage at short circuit V_{SC}

Maximum DC bus voltage of the main circuit (voltage between the P terminal and the N terminal of the IPM) that can perform protective operation in the event of a short circuit when the specified test set temperature and specified control voltage are applied.

If a short circuit occurs at a voltage exceeding this value, protection cannot be performed, and the device may be destroyed.

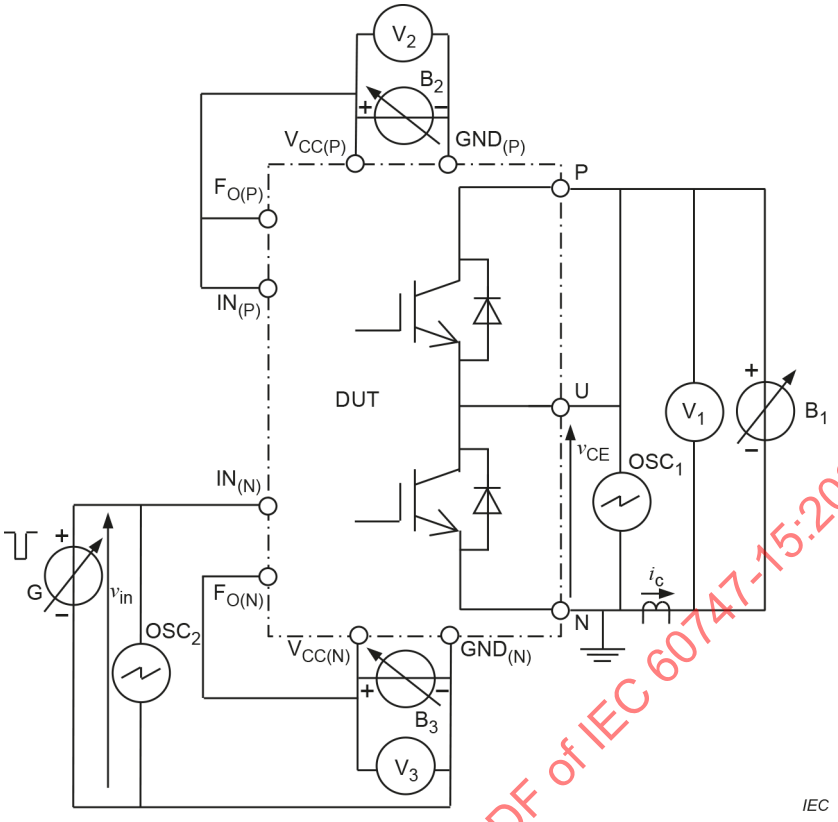
Testing method is shown below.

– Purpose

To confirm that the DUT is protected by the protection function in the event a short circuit and can withstand the short circuit protection operation under the specified conditions.

– Test circuit

Testing circuit is shown in Figure C.4, and the waveforms are shown in Figure C.5.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
OSC_1	Oscilloscope for voltage v_{CE} between collector and emitter observation
OSC_2	Oscilloscope for voltage v_{in} between $IN_{(N)}$ and $GND_{(N)}$ observation

Figure C.4 – Testing circuit for main circuit DC bus voltage at short circuit

– Test procedure

1) Connect the test circuit shown in Figure C.4 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3. Also, apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
4) Apply the ON-signal (longer enough to activate short circuit protection, usually 10 µs or more) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by the Variable pulse voltage source G.
5) Confirm that there are no destruction or abnormalities after the short circuit test.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;

b) Specified main DC bus voltage (between P and N terminal by voltage source B_1);

c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;

d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

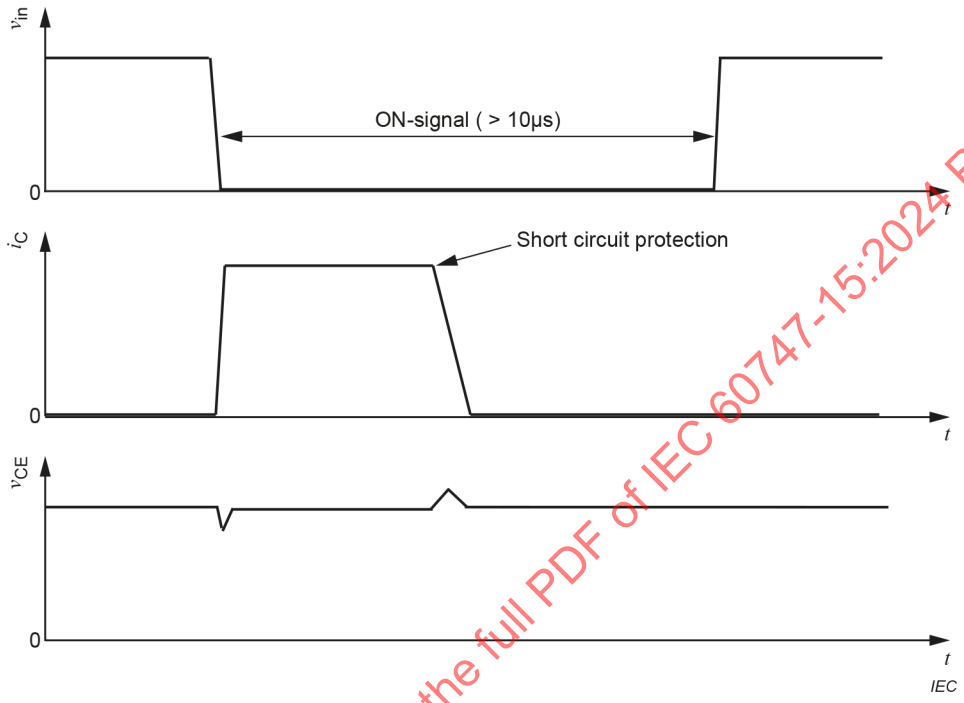


Figure C.5 – Waveforms of short circuit protection function

C.3.2.6 Acceptance defining criteria

All rating tests should be verified to be normal by measuring the characteristics of the IPM control circuit shown in Table C.1 after the tests are completed. The normal characteristic value is not higher than the upper limit USL of the acceptance criteria and is not lower than the lower limit LSL.

Table C.1 – Acceptance defining criteria for the IPM control circuit after rating tests

Subclause	Acceptance defining characteristics	Acceptance criteria
C.3.3.5	Short circuit trip level SC / Over current protection level I_{OC}	SC / I_{OC} > LSL
C.3.3.8	Control circuit under-voltage protection UV / V_{UV}	LSL < UV / V_{UV} < USL
C.3.3.3	Control circuit current I_D / I_{CCP}, I_{CCN}	I_D / I_{CCP}, I_{CCN} < USL
USL: upper specified limit. LSL: lower specified limit.		

C.3.3 Characteristics and measuring method

C.3.3.1 Turn-off times and turn-off switching energy at inductive load

Turn-off times and turn-off switching energy of IPM are defined with starting from the time when the input threshold voltage reached, under the specified measurement set temperature and specified control circuit conditions.

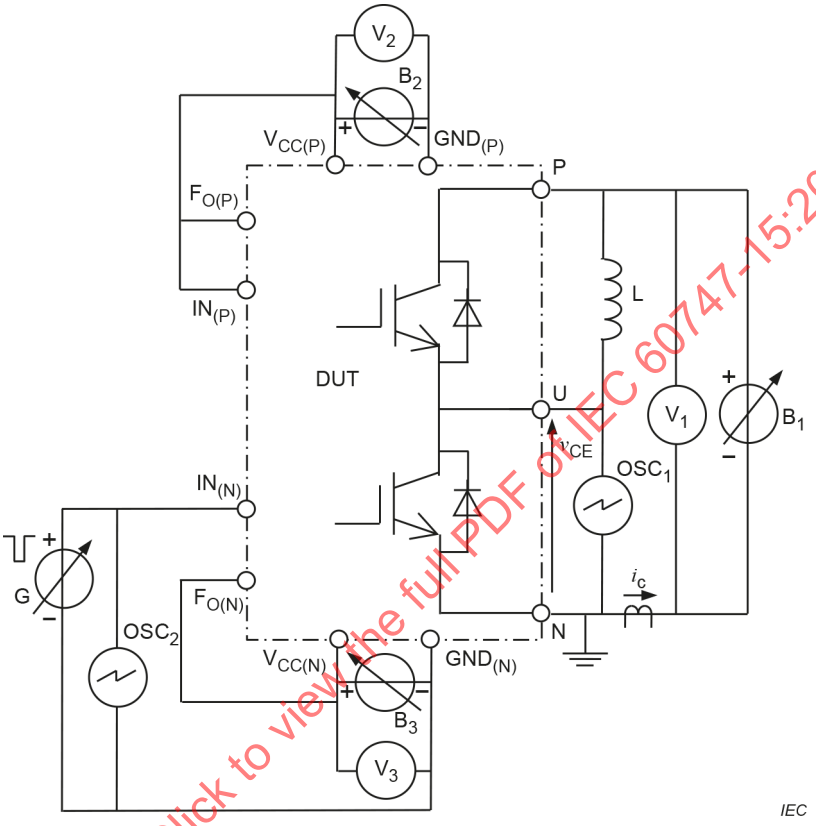
Measurement method is shown below.

– Purpose

To measure the turn-off switching times and turn-off switching energy when an inductive load current is passed through the DUT under the specified conditions.

– Measurement circuit

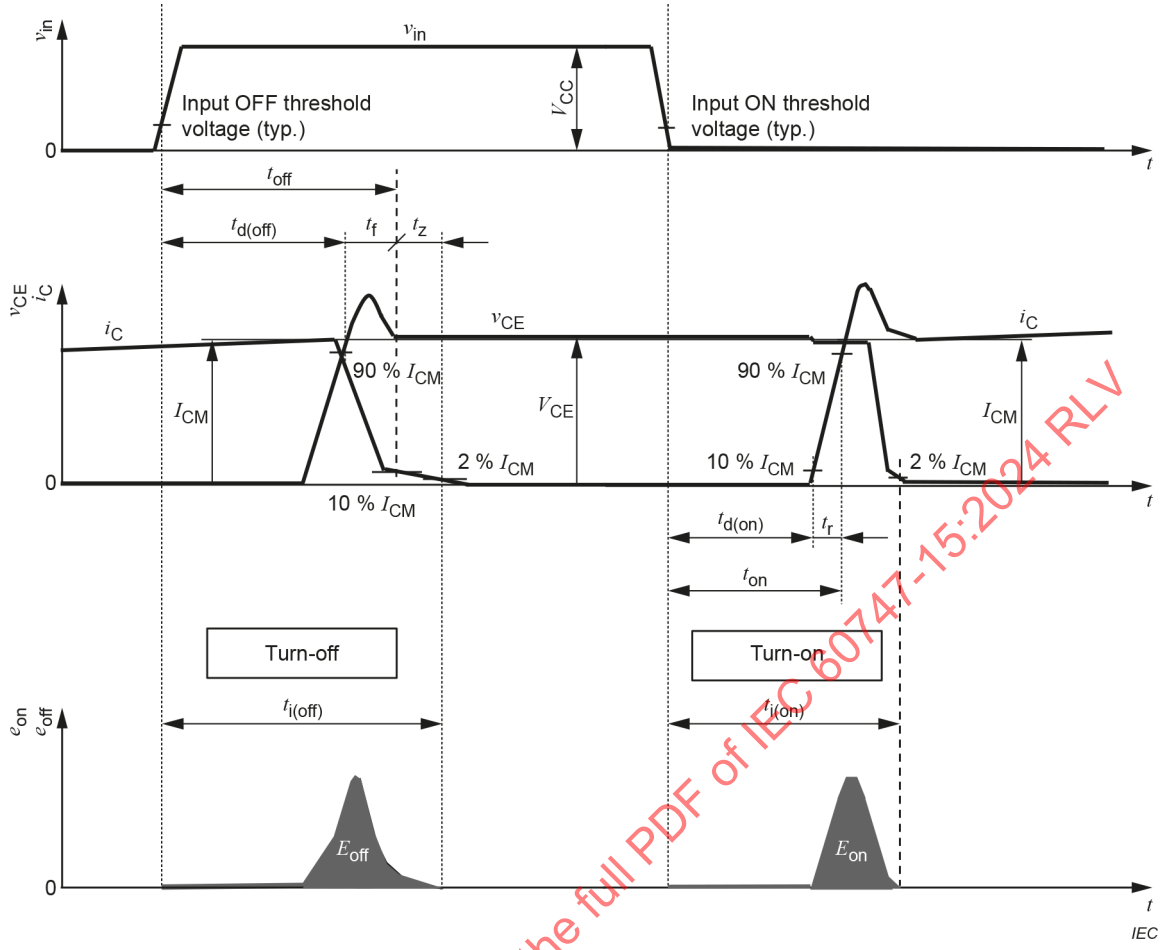
Measurement circuit is shown in Figure C.6, and the waveforms are shown on left side of Figure C.7.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
L	Load inductor
OSC_1	Oscilloscope for voltage between collector and emitter observation
OSC_2	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

Figure C.6 – Measurement circuit for switching times and switching energy at inductive load (lower arm device measurement)



Key

$t_{d(off)}$	Turn-off delay time	$t_{d(on)}$	Turn-on delay time
t_f	Fall time	t_r	Rise time
t_z	Tail time	t_{off}	Turn-off time
E_{off}	Turn-off energy	t_{on}	Turn-on time
$t_{i(off)}$	Integral time for turn-off energy	E_{on}	Turn-on energy
		$t_{i(on)}$	Integral time for turn-on energy

Figure C.7 – Switching waveforms at inductive load

– Measurement procedure

1) Connect the test circuit shown in Figure C.6 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G in order to turn on the IGBT of DUT for the specified period. Adjust the voltage of the variable constant voltage power supply B_1 to raise the collector current flowing through the load inductor L to the specified current. Then, turn off the IGBT to observe the waveforms of the $IN_{(N)}$ terminal and $GND_{(N)}$ terminal voltage v_{in}, collector-emitter voltage v_{CE}, and collector current i_C with the oscilloscope and current sensor.

5) From the observed waveform, find the switching times at turn-on ($t_{d(off)}$, t_f, t_z, t_{off}) shown in Figure C.7, and calculate turn-on switching energy E_{off} which is integrated the product of the collector-emitter voltage v_{CE} and the collector current i_C over the integral time $t_{i(off)}$.

– Specified conditions

a) Collector current I_{CM};

b) Voltage of control circuit power supply B_2, B_3;

c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;

d) Specified main DC bus voltage (between P and N terminal by voltage source B_1);

e) Inductance value of the load inductor L;

f) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.2 Turn-on times and turn-on switching energy at inductive load

Turn-on times and turn-on switching energy of IPM are defined with starting from the time when the input threshold voltage reached, under the specified measurement set temperature and specified control circuit conditions.

Measurement method is shown below.

– Purpose

To measure the turn-on switching times and turn-on switching energy when an induced load current is passed through the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.7, and the waveforms are shown on right side of Figure C.7.

– Measurement procedure

1) Connect the test circuit shown in Figure C.6 to the DUT.

2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.

3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.

4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G in order to turn on the IGBT of DUT for the specified period. Adjust the voltage of the variable constant voltage power supply B_1 to raise the collector current flowing through the load inductor L to the specified current. Turn off the IGBT once and circulate the current through the load inductor L and the freewheeling diode on the opposite arm. Then, turn on the IGBT again by applying second ON-signal pulse in order to observe the waveforms of the $IN_{(N)}$ terminal and $GND_{(N)}$ terminal voltage v_{in}, collector-emitter voltage v_{CE}, and collector current i_C with the oscilloscope and current sensor.

5) From the observed waveform, find the switching times at turn-on ($t_{d(on)}$, t_r, t_{on}) shown in Figure C.7, and calculate turn-on switching energy E_{on} which is integrated the product of the collector-emitter voltage and the collector current i_C over the integral time $t_{i(on)}$.

NOTE By measuring the voltage and current waveforms of the opposite (upper) arm at the time of inductive load turn-on, the reverse recovery time, reverse recovery loss energy, and reverse recovery charge of the freewheeling diode can be measured.

– Specified conditions

a) Collector current I_{CM};

b) Voltage of control circuit power supply B_2, B_3;

c) Specified input signal (double pulse) between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;

d) Specified main DC bus voltage (between P and N terminal by voltage source B_1);

e) Inductance value of the load inductor L;

f) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.3 Control circuit current of upper arm I_D / I_{CCP}, and control circuit current of lower arm I_D / I_{CCN}

The maximum value of the effective current consumed by the control circuit of the IPM in the specified measurement set temperature, the specified control circuit conditions, and the input signal is off or the drive signal to the IGBT is input at the specified frequency.

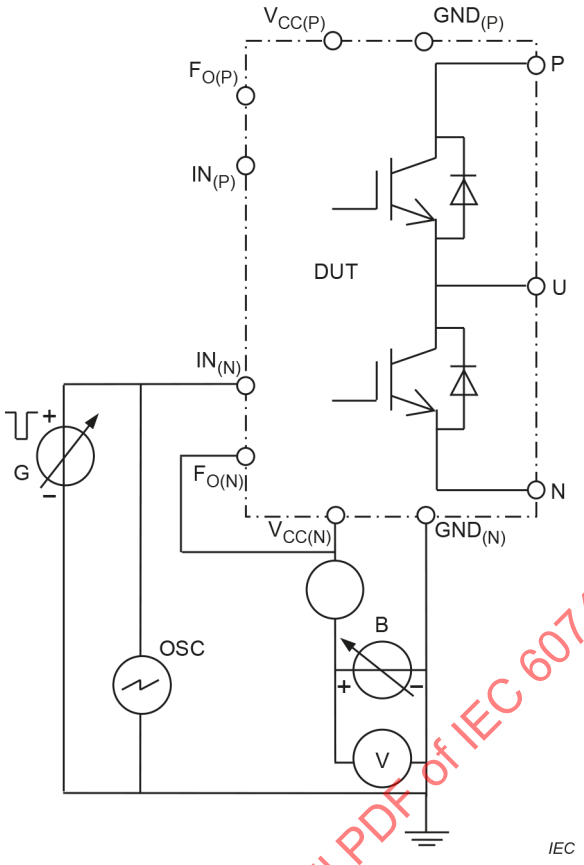
Measurement method as example of lower arm is shown below.

– Purpose

To measure the control circuit current of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.8.



Key

DUT IPM under test

G Variable pulse voltage source

B Power supply voltage source of lower arm control circuit

OSC Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

V Voltmeter for lower arm control circuit power supply observation

A Ammeter for lower arm control circuit power supply observation

Figure C.8 – Measurement circuit for control circuit current

– Measurement procedure

1) Connect the test circuit shown in Figure C.8 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal by the power supply voltage source B, and apply the input signal between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G.
4) Measure the control circuit current by ammeter A.

– Specified conditions

a) Voltage of control circuit power supply B;
b) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.4 Input ON threshold voltage $V_{th(on)}$ / $V_{inth(on)}$, and input OFF threshold voltage $V_{th(off)}$ / $V_{inth(off)}$

Maximum, minimum and typical values of the input ON / OFF threshold voltage to the control circiot for outputting the ON / OFF signal to the IGBT under the specified measurement set temperature and specified control circuit conditions.

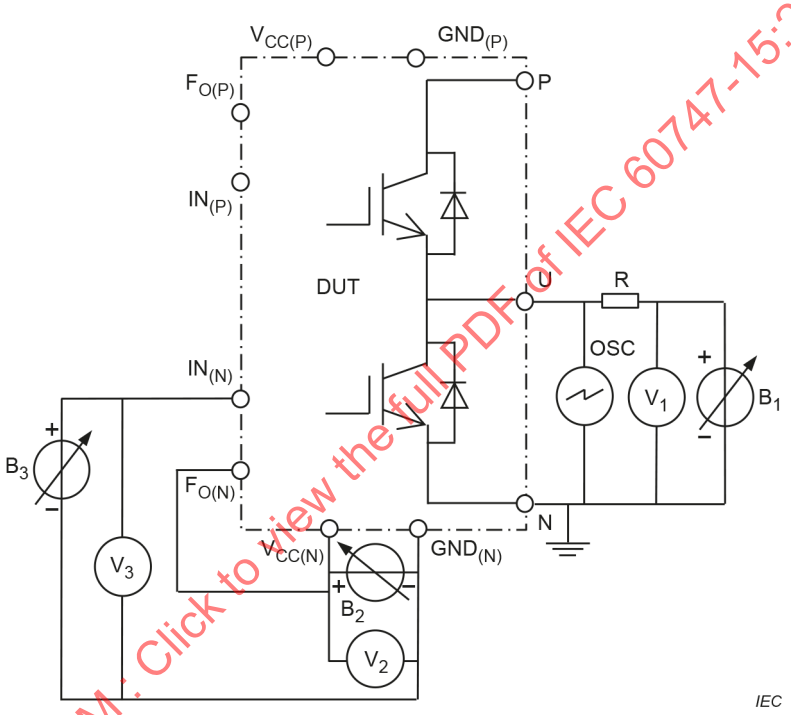
Measurement method as example of lower arm is shown below.

– Purpose

To measure the input ON threshold voltage and input OFF threshold voltage of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.9.



Key

DUT IPM under test

B_1 Power supply voltage source for collector current

B_2 Power supply voltage source of lower arm control circuit

B_3 Voltage source between $IN_{(N)}$ and $GND_{(N)}$

V_1 Voltmeter for main DC bus voltage (between P terminal and N terminal) observation

V_2 Voltmeter for lower arm control circuit power supply observation

V_3 Voltmeter for lower arm input signal observation

R Current limiting resistor

OSC Oscilloscope for voltage between collector and emitter observation

Figure C.9 – Measurement circuit for input threshold voltage

– Measurement procedure for input ON threshold voltage

1) Connect the test circuit shown in Figure C.9 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal by the power supply voltage source B_2.
4) Decrease voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal gradually, then, measure the voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by voltmeter V_3 when collector-emitter voltage go down to specified value.

– Measurement procedure for input OFF threshold voltage

After measurement of input ON threshold voltage, increase voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal gradually, then, measure the voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by voltmeter V_3 when collector-emitter voltage go up to voltage of B_1.

– Specified conditions

a) Voltage of B_1 for collector current supplying;
b) Voltage of control circuit power supply B_2;
c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.5 Over current protection level I_{OC} / Short circuit trip level SC

Minimum trip level for over current protection or short-circuit protection under the specified measurement set temperature and specified control circuit conditions.

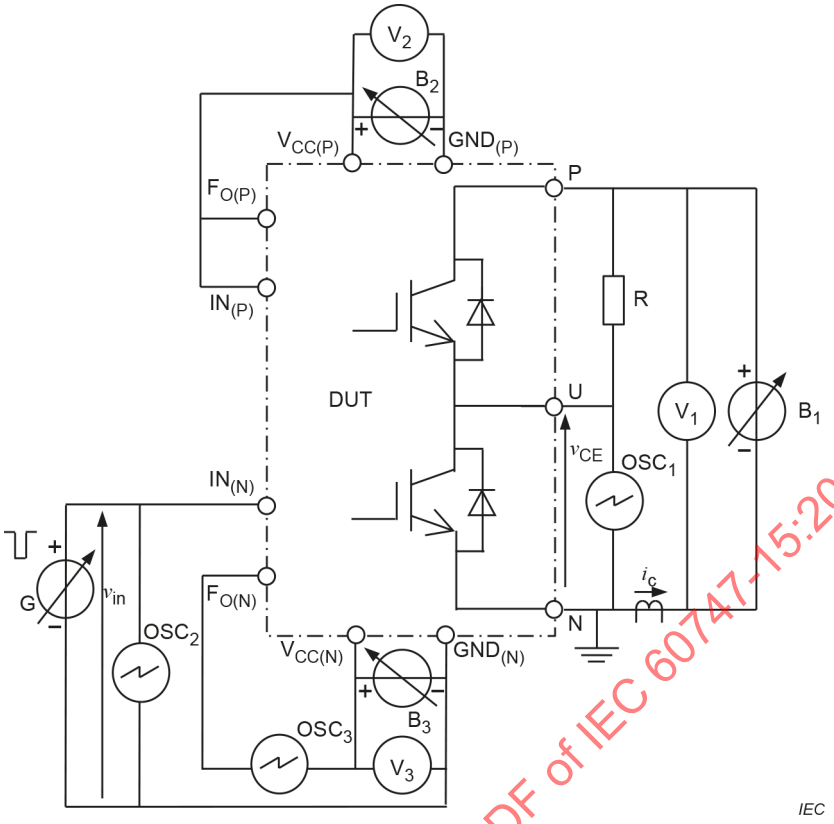
Measuring method as example of lower arm is shown below.

– Purpose

To measure the over current protection level / short circuit trip level of the DUT under the specified conditions.

– Measurement circuit

Measuring circuit is shown in Figure C.10, and waveforms during the protection operation are shown in Figure C.11.



Key

DUT IPM under test

B_1 Power supply voltage source for collector current

B_2 Power supply voltage source of upper arm control circuit

B_3 Power supply voltage source of lower arm control circuit

V_1 Voltmeter for main DC bus voltage (between P terminal and N terminal) observation

V_2 Voltmeter for upper arm control circuit power supply observation

V_3 Voltmeter for lower arm control circuit power supply observation

G Variable pulse voltage source

R Load resistor

OSC_1 Oscilloscope for voltage between collector and emitter observation

OSC_2 Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

OSC_3 Oscilloscope for Fault / Alarm output signal observation

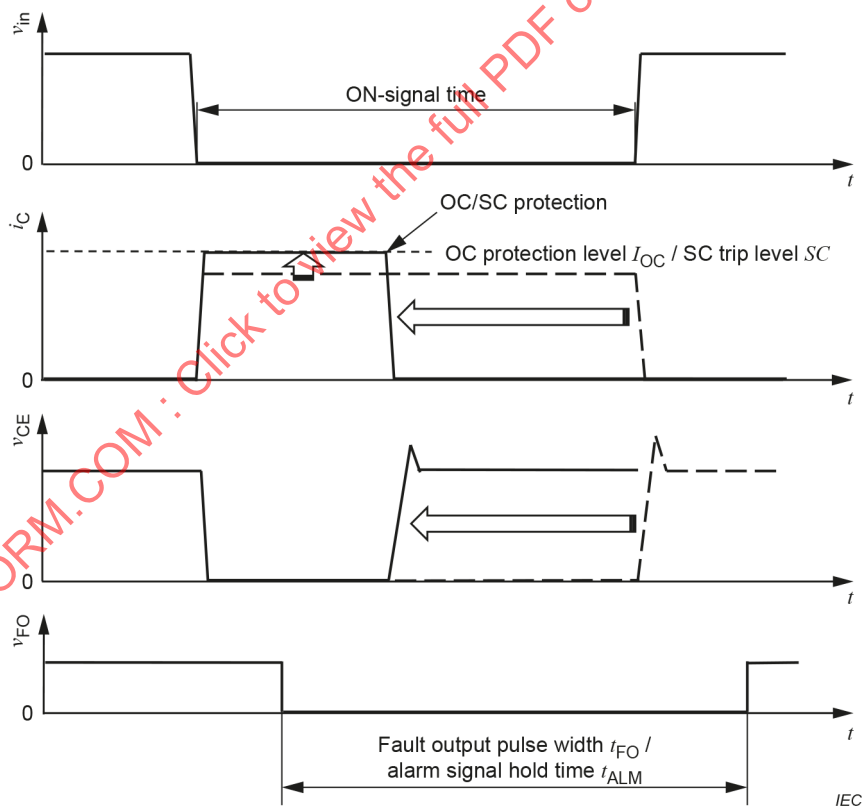
Figure C.10 – Measuring circuit for over current protection level/short circuit trip level

– Measurement procedure for input ON threshold voltage

1) Connect the test circuit shown in Figure C.10 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G, and increase gradually the voltage of the variable constant voltage power supply B_1 to raise the collector current until the protection function operation.
5) Then, measure the collector current just before protection operation, fault output pulse width or alarm time, and fault or alarm output signal v_{FO} simultaneously.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;
b) Input ON-signal (longer enough than t_{dOC} / $t_{off(SC)}$);
c) Voltage of B_1 for collector current supplying (< V_{SC}) with adjusting R_0;
d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.



NOTE The fault or alarm output signal can be measured by current I_{FO} observation like Figure C.3 or current sensor with oscilloscope instead of voltage v_{FO} observation. In that case, the i_{FO} waveform is inverse shape of v_{FO}.

Figure C.11 – Waveforms during over current protection / short circuit protection

C.3.3.6 Over current protection delay time t_{doc} / Short circuit current delay time $t_{off(SC)}$

Typical value of collector turn-off delay time during over current protection or short circuit protection operation under the specified measurement set temperature and specified control circuit conditions.

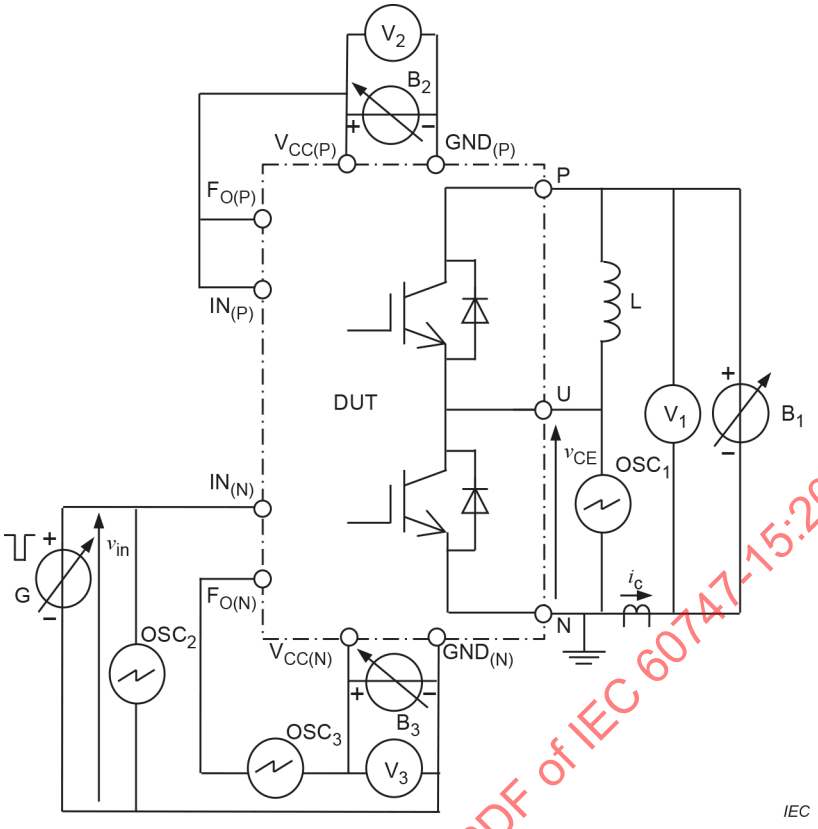
Measurement method as example of lower arm is shown below.

– Purpose

To measure the over current protection delay time t_{dOC} / short circuit current delay time $t_{off(SC)}$ of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.12, and waveforms during the protection operation are shown in Figure C.13.



Key

DUT IPM under test

B_1 Power supply voltage source for collector current

B_2 Power supply voltage source of upper arm control circuit

B_3 Power supply voltage source of lower arm control circuit

V_1 Voltmeter for main DC bus voltage (between P terminal and N terminal) observation

V_2 Voltmeter for upper arm control circuit power supply observation

V_3 Voltmeter for lower arm control circuit power supply observation

G Variable pulse voltage source

L Load inductor

OSC_1 Oscilloscope for voltage between collector and emitter observation

OSC_2 Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation

OSC_3 Oscilloscope for fault / alarm output signal observation

Figure C.12 – Measurement circuit for over current protection delay time/Short circuit current delay time

– Measurement procedure

1) Connect the test circuit shown in Figure C.12 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
5) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G, and increase gradually the ON-signal pulse width to raise the collector current until the protection function operation.
6) Then, measure the time from when the over current protection level or the short circuit trip level is exceeded until the fault output signal starts to be output.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;
b) Specified main DC bus voltage (between P and N terminal by voltage source B_1);
c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

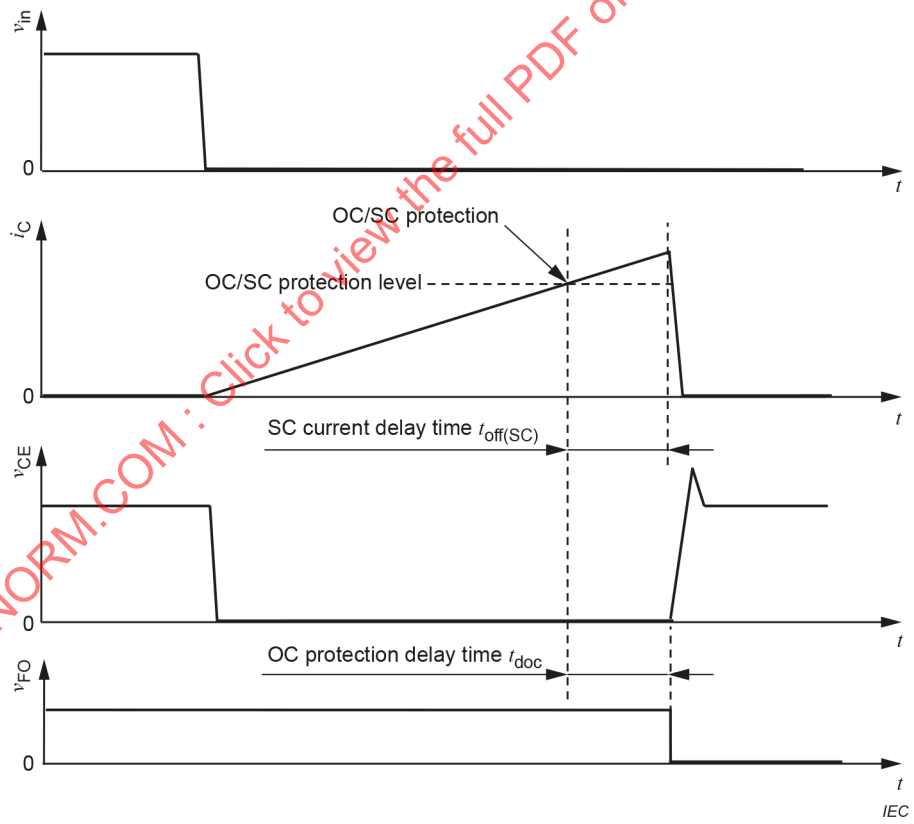


Figure C.13 – Waveforms of protection delay time during over current protection / short circuit protection

C.3.3.7 Over temperature protection OT / overheating protection temperature level T_{jOH}, and over temperature protection hysteresis $OT_{(hys)}$ / overheating protection hysteresis T_{jH}

Typical or minimum value of the over temperature protection level or overheating protection trip level, and the over temperature protection hysteresis or overheating protection hysterisis under the specified measurement set temperature and specified control circuit conditions.

Measurement method as example of lower arm is shown below.

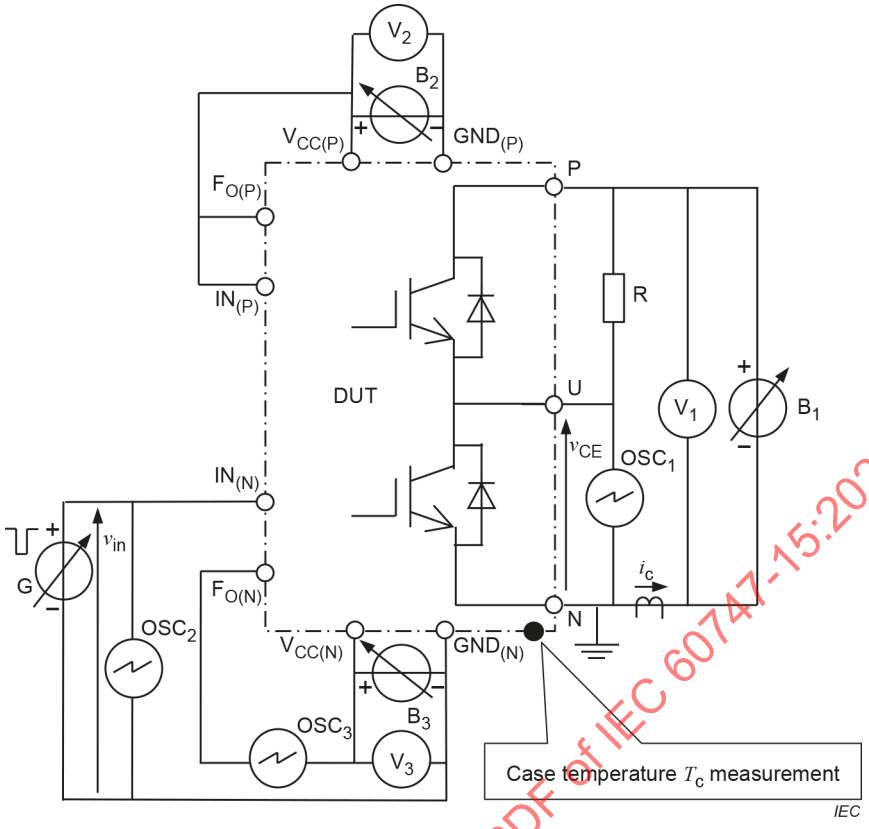
– Purpose

To measure the over temperature protection OT / overheating protection temperature level T_{jOH}, and the over temperature protection hysteresis $OT_{(hys)}$ / overheating protection hysteresis T_{jH} of the DUT under the specified conditions.

The thermal protection trip level and reset level measurement exceeds the maximum rated junction temperature, so the product structure may be destroyed.

– Measurement circuit

Measurement circuit is shown in Figure C.14, and waveforms during the protection operation are shown in Figure C.15.



Key

DUT	IPM under test
B_1	Power supply voltage source for collector current
B_2	Power supply voltage source of upper arm control circuit
B_3	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V_2	Voltmeter for upper arm control circuit power supply observation
V_3	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
R	Load resistor
OSC_1	Oscilloscope for voltage between collector and emitter observation
OSC_2	Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation
OSC_3	Oscilloscope for fault / alarm output signal observation

Figure C.14 – Measurement circuit for over temperature protection and its hysteresis

– Measurement procedure

1) Connect the test circuit shown in Figure C.14 to the DUT.
2) Set the DUT on a hot plate or constant temperature chamber with large enough heat capacity enable to adjust case temperature.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
5) Input the ON / OFF signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G, and set the collector current value (pulse width duty) sufficiently small so that the virtual junction temperature does not rise.
6) Adjust setting of the hot plate or constant temperature chamber to raise the case temperature T_c slowly (dT/dt is 1 °C/min. or around), and measure the case temperature when the collector current is cut off or a fault output signal is output. The frequency of the input signal is short enough for the case temperature Tc changes, the guideline is 1 Hz or around.
7) After measuring the over temperature protection or overheating protection temperature level, lower the case temperature T_c slowly (dT/dt is 1 °C/min. or around), and measure the case temperature when the collector current flows again. The difference between this temperature and the over temperature protection or overheating protection temperature level is the overheating protection hysteresis $OT_{(hys)}$ / T_{jH}.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3;
b) Main DC bus voltage (between P and N terminal by voltage source B_1);
c) Temperature of the hot plate or constant temperature chamber (the temperature is raised up until overheat protection function is activated);
d) Collector current.

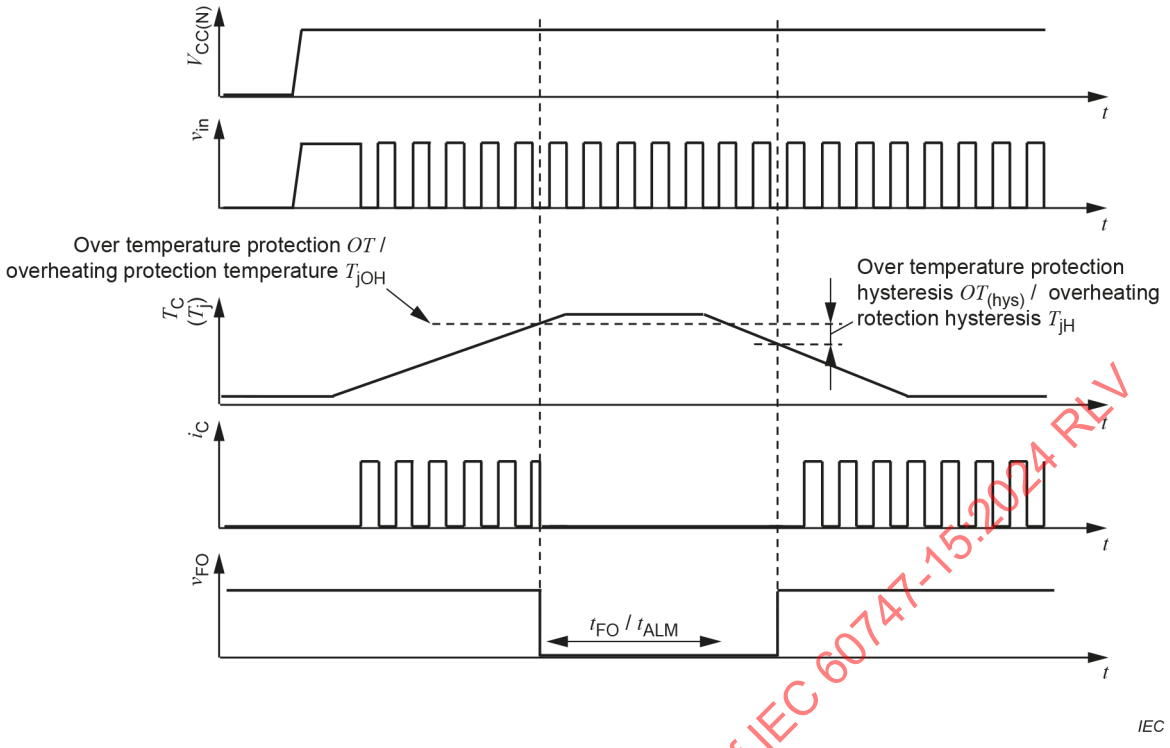


Figure C.15 – Waveforms during the overheating protection operation and the fault output

C.3.3.8 Control circuit under-voltage protection UV / Under-voltage protection level V_{UV}, control circuit under-voltage protection reset level UV_r / Under-voltage protection hysteresis V_H, and fault output pulse width t_{FO} / alarm signal hold time t_{ALM}

Maximum, minimum and typical values of the control circuit under-voltage protection trip level, the control circuit under-voltage protection reset level or the control circuit under-voltage protection hysteresis, and the fault output pulse width or the alarm signal hold time under the specified measurement set temperature and specified control circuit conditions.

Measurement method as example of lower arm is shown below.

– Purpose

  To measure the control circuit under-voltage protection trip level, reset level or protection hysteresis, and fault output pulse width or alarm signal hold time of the DUT under the specified conditions.

– Measurement circuit

  Measurement circuit is same as shown in Figure C.10, and waveforms during the protection operation are shown in Figure C.16.

– Measurement procedure

1) Connect the test circuit shown in Figure C.10 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2, and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3.
4) Apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B_1.
5) Input the ON / OFF signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G and set the collector current value (pulse width duty) sufficiently small so that the virtual junction temperature does not rise.
6) Decrease voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ slowly from specified value, and measure the control circuit power supply voltage by voltmeter V_3 when the collector current is cut off or a fault output signal is output. The frequency of the input signal is short enough for the voltage changes of B_3.
7) After measuring the under-voltage protection trip level, increase the voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ slowly, and measure the control circuit power supply voltage (reset level) by voltmeter V_3 when the collector current flows again.

– Specified conditions

a) Voltage of control circuit power supply B_2, B_3 (the voltage of B_3 is decreased until protection function is activated);
b) Main DC bus voltage (between P and N terminal by voltage source B_1);
c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj};
d) Collector current.

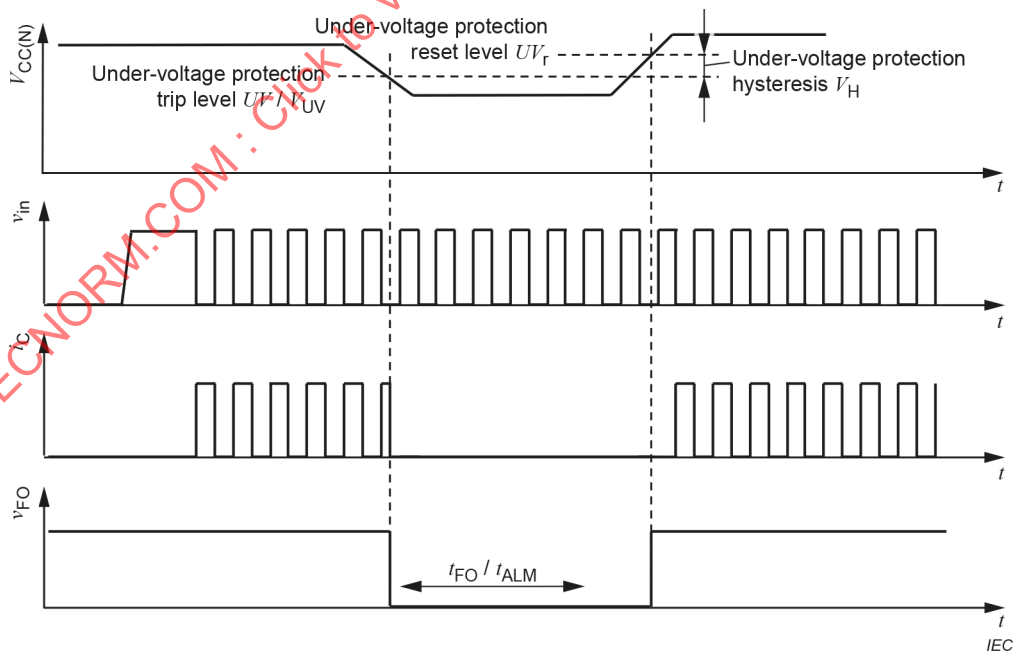


Figure C.16 – Waveforms during the under-voltage protection operation and the fault output

C.3.3.9 Fault output current $I_{FO(H)}$ (during unprotection), $I_{FO(L)}$ (during protection), and alarm signal current limiting resistance value R_{ALM}

Maximum and typical values of the fault output current during no protection operation and the fault output current during the protection operation under the specified measurement set temperature and specified control circuit conditions.

The fault or alarm output signal current $I_{FO(L)}$ is typical or maximum value usually. On the other hand, the fault or alarm output signal current during no protection function operation is expressed with letter symbol of $I_{FO(H)}$, maximum value is required usually.

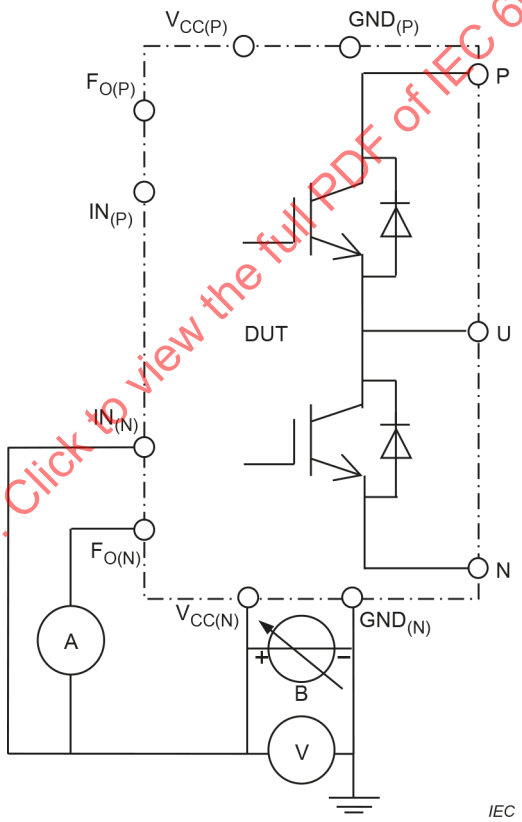
Measurement method as example of lower arm is shown below.

– Purpose

To measure the fault output current $I_{FO(H)}$, $I_{FO(L)}$, and the alarm signal current limiting resistance value R_{ALM} of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.17.



Key

DUT IPM under test

B Power supply voltage source of lower arm control circuit

V Voltmeter for lower arm control circuit power supply observation

A Ammeter for fault/alarm output current

Figure C.17 – Measurement circuit for fault output current

– Measurement procedure

1) Connect the test circuit shown in Figure C.17 to the DUT.
2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal, and measure the $I_{FO(H)}$ current flowing through the $F_{O(N)}$ terminal by ammeter A or current sensor with oscilloscope. Since the fault output current $I_{FO(L)}$ is the current during the protection operation, it is measured during the over current protection level / short circuit trip level measurement. See C.3.3.5. Use an ammeter or current sensor with oscilloscope instead of OSC_3 in Figure C.10.
4) Since the alarm signal current limiting resistance value R_{ALM} is not measured directly, it is calculated by the control circuit power supply voltage value (voltage value of B) divided by the fault output current $I_{FO(L)}$.

– Specified conditions

a) Voltage of control circuit power supply B;
b) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

C.3.3.10 Common mode noise withstand capability

Maximum or typical allowable noise withstand capability that does not malfunction with respect to common mode noise to commercial input power supplies.

Measurement method as example of lower arm is shown below.

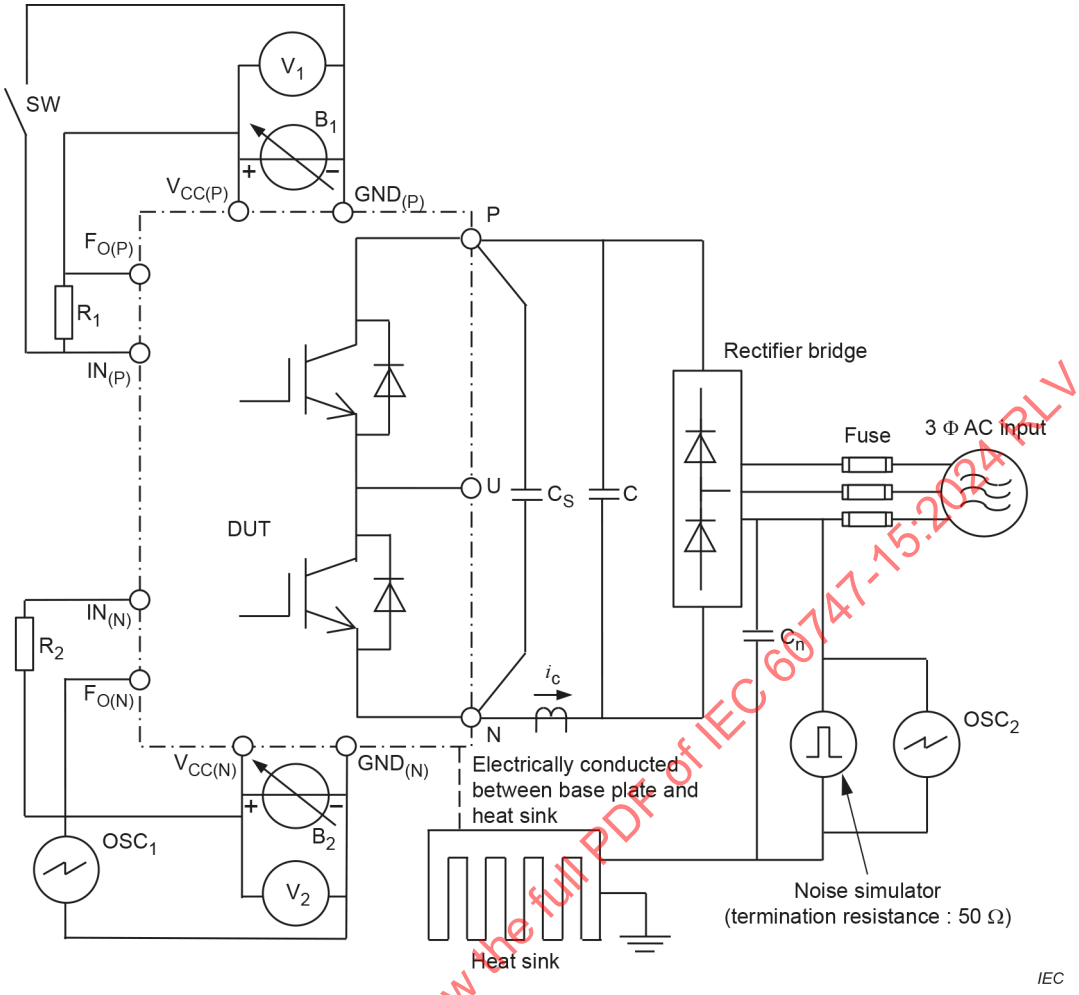
– Purpose

To measure the noise withstand capability of the common mode noise voltage applied to the commercial input power supply so that the DUT does not erroneously turn on or output fault signal under the specified conditions.

NOTE If the IPM operates incorrectly, it can cause a major obstacle, such as a short circuit accident. On the other hand, even if the IPM erroneously turns off, it recovers when the input PWM signal is turned off, and in many cases it does not pose a critical obstacle to the load output. Therefore, the description of the measurement method for erroneous off is omitted.

– Measurement circuit

Measurement circuit is shown in Figure C.18, and waveforms during the operation are shown in Figure C.19. The control circuit of the upper arm that are not measured are always ON, and the lower arm to be measured is always OFF. Also, both ends of the DC bus capacitor C and the snubber capacitor C_S are connected to the P and N terminal of the DUT.



Key

DUT	IPM under test
B_1	Power supply voltage source of upper arm control circuit
B_2	Power supply voltage source of lower arm control circuit
V_1	Voltmeter for upper arm control circuit power supply observation
V_2	Voltmeter for lower arm control circuit power supply observation
R_1	Upper arm input signal pull-up resistor
R_2	Lower arm input signal pull-up resistor
SW	ON fixing switch
C	DC bus capacitor
C_S	Snubber capacitor
Cn	Grounding capacitor
OSC_1	Oscilloscope for lower arm control circuit fault output observation
OSC_2	Oscilloscope for noise voltage waveform observation

Figure C.18 – Measurement circuit for common mode noise withstand capability

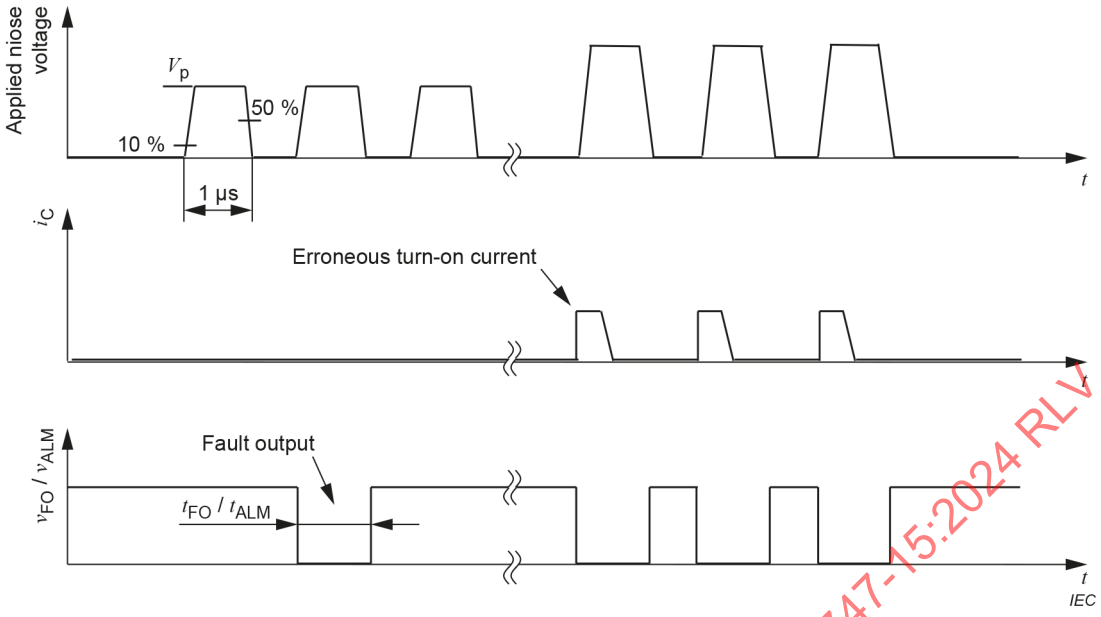


Figure C.19 – Waveforms during the common mode noise withstand capability measurement

– Measurement procedure

1) Pull up the $IN_{(N)}$ terminal to $V_{CC(N)}$ through the pull-up resistor R_2 so that the lower arm of the DUT does not turn on. The pull-up resistor shall have a resistance value equivalent to that in actual use. Usually, 20 kΩ or around is often used.
2) Pull up the $IN_{(P)}$ terminal to $V_{CC(P)}$ through the pull-up resistor R_1 so that the upper arm of the DUT turns on always. Also, pull up the $F_{O(P)}$ terminal of the upper arm to $V_{CC(P)}$ to prevent malfunction. Provide a circuit to turn on with the switch SW.
3) For the upper arm control circuit power supply voltage source B_1 and the lower arm control circuit power supply voltage source B_2, use isolation transformers or the like to reduce stray capacitance to ground, and set them to the specified values $V_{CC(P)}$ and $V_{CC(N)}$, respectively. Insulate the oscilloscope OSC_1 and OSC_2 with isolation transformers or the like as well.
4) Turn on the ON fixing switch SW, and always turn the upper arm that is not measured.
5) Turn on the 3Φ AC input. If necessary, use a reactor or sliding voltage regulator so that the rectifier bridge will not be destroyed by the inrush surge current.
6) Apply noise with the noise simulator. Set the noise pulse width to 1 µs, set V_p to the specified value, and confirm the set value with the oscilloscope OSC_2. The fall time depends on the specified value of the noise simulator.
7) Measure the collector current i_C on the lower arm and the fault output voltage $v_{FO(N)}$ / v_{ALM} and confirm that there is no erroneous fault output or malfunction current within the specified noise applying time. In case of malfunction, over current due to short circuit through P terminal to N terminal flows and is quickly cut off by the protection function, so it is desirable to connect the snubber capacitor C_S.
8) Increase V_p as necessary and confirm the V_p at which the malfunction current or fault output occurs. When the measurement is completed, turn off all the power supplies in the reverse order of start-up.
9) Connect the output polarities of the noise simulator in reverse and perform steps d) to h). If necessary, perform steps c) to i) for other phases of the 3Φ AC input. However, it is not possible to apply noise to the ground phase.

– Specified conditions

a) Pull-up resistor R_1, R_2;

b) Voltage of control circuit power supply B_1, B_2;

c) Voltage of 3Φ AC input;

d) Voltage V_p of the noise simulator;

e) Ambient or case or virtual junction temperature T_a or T_c or T_{vj}.

Bibliography

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IEC 61287-1:2014, *Railway applications – Power converters installed on board rolling stock – Part 1: Characteristics and test methods*

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SOMMAIRE

COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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DISPOSITIFS À SEMICONDUCTEURS –

Partie 15: Dispositifs discrets – Dispositifs de puissance à semiconducteurs isolés

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L'IEC 60747-15 a été établie par le sous-comité 47E: Dispositifs discrets à semiconducteurs, du comité d'études 47 de l'IEC: Dispositifs à semiconducteurs. Il s'agit d'une Norme internationale.

Cette troisième édition annule et remplace la deuxième édition parue en 2010. Cette édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) les modules de puissance à semiconducteurs intelligents (IPM, Intelligent Power semiconductor Module), qui étaient auparavant exclus des première et deuxième éditions, sont désormais inclus dans le présent document (Annexe C);
b) la résistance thermique est décrite pour chaque interrupteur (6.2.4);
c) ajout d'un essai d'isolement entre le capteur de température et les bornes, en cas d'accord avec l'utilisateur (6.1.2).

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
47E/832/FDIS	47E/844/RVD

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

La version française de la norme n'a pas été soumise au vote.

Ce document a été rédigé selon les Directives ISO/IEC, Partie 2, il a été développé selon les Directives ISO/IEC, Partie 1 et les Directives ISO/IEC, Supplément IEC, disponibles sous www.iec.ch/members_experts/refdocs. Les principaux types de documents développés par l'IEC sont décrits plus en détail sous www.iec.ch/publications.

La présente Norme internationale est à utiliser conjointement avec l'IEC 60747-1:2006 et son Amendement 1:2010.

Une liste de toutes les parties de la série IEC 60747, publiées sous le titre général *Dispositifs à semiconducteurs*, se trouve sur le site Web de l'IEC.

Le comité a décidé que le contenu de ce document ne sera pas modifié avant la date de stabilité indiquée sur le site Web de l'IEC sous webstore.iec.ch dans les données relatives au document recherché. À cette date, le document sera:

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- révisé.

DISPOSITIFS À SEMICONDUCTEURS –

Partie 15: Dispositifs discrets – Dispositifs de puissance à semiconducteurs isolés

1 Domaine d'application

Le présent document spécifie les exigences relatives aux dispositifs de puissance à semiconducteurs isolés. Ces exigences s'ajoutent à celles qui figurent dans d'autres parties de l'IEC 60747 pour les dispositifs de puissance non isolés correspondants et dans des parties de l'IEC 60748 pour les circuits intégrés.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

IEC 60068-2-1:2007, *Essais d'environnement – Partie 2-1: Essais – Essai A: Froid*

IEC 60270:2015, *Techniques des essais à haute tension – Mesures des décharges partielles*

IEC 60664-1:2020, *Coordination de l'isolement des matériels dans les réseaux d'énergie électrique à basse tension – Partie 1: Principes, exigences et essais*

IEC 60721-3-3:2019, *Classification des conditions d'environnement – Partie 3-3: Classification des groupements des agents d'environnement et de leurs sévérités – Utilisation à poste fixe, protégé contre les intempéries*

IEC 60747-1:2006 *Dispositifs à semiconducteurs – Partie 1: Généralités*
IEC 60747-1:2006/AMD1:2010

IEC 60747-2:2016, *Dispositifs à semiconducteurs – Partie 2: Dispositifs discrets – Diodes de redressement*

IEC 60747-6:2016, *Dispositifs à semiconducteurs – Partie 6: Dispositifs discrets – Thyristors*

IEC 60747-7:2019, *Dispositifs à semiconducteurs – Dispositifs discrets – Partie 7: Transistors bipolaires*

IEC 60747-8:2021, *Semiconductor devices – Part 8: Field-effect transistors (disponible en anglais seulement)*

IEC 60747-9:2019, *Dispositifs à semiconducteurs – Partie 9: Dispositifs discrets – Transistors bipolaires à grille isolée (IGBT)*

IEC 60748 (toutes les parties), *Dispositifs à semiconducteurs – Circuits intégrés*

IEC 60749-5:2017, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 5: Essai continu de durée de vie sous température et humidité avec polarisation*

IEC 60749-6:2017, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 6: Stockage à haute température*

IEC 60749-10:2003, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 10: Chocs mécaniques*

IEC 60749-12:2017, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 12: Vibrations, fréquences variables*

IEC 60749-15:2020, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 15: Résistance à la température de brasage pour dispositifs par trous traversants*

IEC 60749-21:2011, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 21: Brasabilité*

IEC 60749-25:2003, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 25: Cycles de température*

IEC 60749-34:2010, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 34: Cycles en puissance*

3 Termes et définitions

Pour les besoins du présent document, les termes et définitions suivants s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse https://www.electropedia.org/
- ISO Online browsing platform: disponible à l'adresse https://www.iso.org/obp

3.1
dispositif de puissance à semiconducteur isolé
dispositif de puissance à semiconducteurs contenant un isolant électrique intégral entre la surface ou l'embase de refroidissement et tous les éléments de circuit isolés

3.2
parties constitutives du dispositif de puissance à semiconducteur isolé

3.2.1
interrupteur
tout composant qui réalise une fonction de commutation dans un circuit électrique, par exemple diode, thyristor, transistor à effet de champ métal-oxyde-semiconducteurs (MOSFET, Metal-Oxide-Semiconductor Field-Effect Transistor), etc.

Note 1 à l'article: Un interrupteur peut être une connexion parallèle ou en série de plusieurs puces avec une seule fonctionnalité.

3.2.2
embase
partie du boîtier comportant une surface de refroidissement qui transfère la chaleur de l'intérieur vers l'extérieur

3.2.3
borne principale
borne du circuit de puissance comportant un potentiel élevé et parcourue par le courant principal

Note 1 à l'article: La borne principale peut comprendre plus d'un connecteur physique.

3.2.4
borne de commande
borne apte, en courant faible, à la fonction de commande et à laquelle sont appliqués les signaux de commande externes ou de laquelle proviennent les paramètres de détection

3.2.4.1
borne de commande haute tension
borne connectée électriquement à un élément de circuit isolé, mais parcourue uniquement par le courant faible pour les fonctions de commande

Note 1 à l'article: Les exemples incluent les shunts de courant et les bornes d'un capteur comportant le potentiel élevé des bornes principales.

3.2.4.2
borne de commande basse tension
borne comportant une fonction de commande et isolée des bornes de commande haute tension

Note 1 à l'article: Les exemples incluent les bornes des capteurs de température isolés et les entrées des circuits d'attaque à grille isolée, etc.

3.2.5
couche d'isolant
partie intégrée au boîtier du dispositif qui isole toute partie dont le potentiel est élevé de la surface de refroidissement ou du dissipateur externe et de tout élément de circuit isolé

3.3
courant de crête de non-rupture de boîtier
courant de crête, qui ne conduit pas à une rupture du boîtier, avec rejet de particules massives et de plasma dans des conditions spécifiques

3.4
matériau d'interface thermique
matériau conducteur de chaleur placé entre l'embase et le dissipateur externe

4 Symboles littéraux

4.1 Généralités

Les symboles littéraux sont définis à l'Article 4 de l'IEC 60747-1:2006.

4.2 Symboles et indices supplémentaires

p parasite

t borne

isol isolement

4.3 Liste de symboles littéraux

4.3.1 Tensions et courants

Courant de borne	I_{teff}
Tension d'isolement	V_{isol}
Tension d'apparition de décharge partielle	V_i
Tension d'extinction de décharge partielle	V_e
Courant de fuite d'isolement	I_{isol}

4.3.2 Symboles mécaniques

Couple de serrage des vis du dissipateur	M_s
Couple de serrage des vis des bornes	M_t
Force de serrage	F
Accélération dans chacun des 3 axes (x, y, z)	a
Masse	m
Planéité du boîtier (embase)	e_c
Planéité de la surface du dissipateur	e_s
Rugosité du boîtier (embase)	R_{Zc}
Rugosité de la surface du dissipateur	R_{Zs}
Épaisseur du matériau d'interface thermique (boîtier – dissipateur)	$d_{(c\text{-}s)}$

4.3.3 Autres symboles

Inductance parasite, effective entre bornes et puces	L_p
Capacité parasite entre les bornes et la surface de refroidissement (boîtier, embase, masse)	C_p
Résistance du fil entre la borne X et la connexion interne au dispositif x'	r_{xx}
Température de borne	T_t
Nombre de cycles de puissance en charge jusqu'à défaillance d'un pourcentage p d'une population de dispositifs	$N_{f;p}$

5 Valeurs assignées (valeurs limites) et caractéristiques essentielles

5.1 Généralités

Il convient que les dispositifs de puissance à semiconducteurs isolés soient spécifiés comme des dispositifs évalués et garantis au niveau de leur boîtier ou de leur dissipateur. Il convient que les valeurs assignées et les caractéristiques soient établies à une température de 25 °C ou une autre température plus élevée spécifiée. Les exigences pour plusieurs dispositifs ayant une encapsulation commune sont décrites en 5.12 dans l'IEC 60747-1:2006.

5.2 Valeurs assignées (conditions limites)

5.2.1 Tension d'isolement ou tension d'essai d'isolement (V_{isol})

Valeur efficace ou continue maximale entre les bornes principales et les bornes de commande haute tension d'un côté et les bornes de commande basse tension (le cas échéant) et l'embase de l'autre côté pour une durée spécifiée.

5.2.2 Courant de crête de non-rupture de boîtier (le cas échéant)

Valeur maximale pour chaque borne principale qui n'entraîne pas l'éclatement du boîtier ou un dégagement de plasma et de particules.

5.2.3 Courant de borne (I_{teff}) (le cas échéant)

Valeur efficace maximale du courant qui traverse la borne principale dans les conditions spécifiées au couple de serrage, M_t, minimal, et à la température de borne maximale admissible ($T_{tmax} = T_{stg}$ ou $T_{tmax} \leq T_{vjmax}$).

5.2.4 Températures

5.2.4.1 Température de brasage (T_{bras}) (le cas échéant)

Température maximale de brasage, T_{bras}, pendant le processus de brasage, pendant un temps d'exécution du brasage, t_{bras}, spécifié.

5.2.4.2 Température de stockage (T_{stk})

Températures de stockage minimale et maximale.

5.2.5 Valeurs mécaniques assignées

5.2.5.1 Couple de serrage des vis du dissipateur (M_s)

Couple de serrage minimal et maximal qui doit être appliqué aux vis de fixation du dissipateur.

5.2.5.2 Couple de serrage des vis de bornes (M_t)

Couple de serrage minimal et maximal qui doit être appliqué aux bornes à vis.

5.2.5.3 Force de serrage (F)

Force de serrage minimale et maximale pour les dispositifs montés par pression, à fixation par agrafes, qui doit être appliquée au dispositif de contact par pression isolée.

5.2.5.4 Force de traction sur les bornes (F_t)

Force maximale.

5.2.5.5 Accélération (a)

Valeur maximale dans chaque axe (x, y, z).

5.2.5.6 Planéité de la surface du dissipateur (e_S) (le cas échéant)

Écart maximal de planéité concernant la surface du dissipateur sur l'ensemble de la zone de montage.

5.2.5.7 Rugosité de la surface du dissipateur (R_{Zs}) (le cas échéant)

Rugosité maximale de la surface du dissipateur sur l'ensemble de la zone de montage.

5.2.6 Valeurs climatiques assignées (le cas échéant)

Les valeurs limites des paramètres d'environnement pour l'application finale sont les suivantes:

– température ambiante;
– humidité;
– vitesse et pression d'air;
– irradiation du soleil et d'autres sources de chaleur;
– substances actives mécaniques;
– substances actives chimiques;
– problèmes biologiques.

Elles doivent être décrites dans les classes spécifiées dans l'IEC 60721-3-3:2019, Tableau 1.

5.3 Caractéristiques

5.3.1 Caractéristiques mécaniques

5.3.1.1 Distance de ligne de fuite sur la surface (d_s)

Valeur minimale de la distance sur la surface du matériau isolant du dispositif entre les bornes de différents potentiels et l'embase.

NOTE 1 L'IEC 60112:2020 (détails sur l'indice de résistance au cheminement "IRC") et l'IEC 60664-1:2020, 5.2, s'appliquent.

NOTE 2 Des intervalles d'air entre une surface en plastique et du métal relié à la masse ou entre des bornes de polarité opposée inférieure à 1,0 mm (pour un degré de pollution 2), ou 1,5 mm (degré de pollution 3) raccourcissent considérablement l'estimation de la ligne de fuite (pour les détails, voir IEC 60664-1:2020, Exemples). Ceci est important si de la poussière, de l'humidité ou des salissures commencent à recouvrir la surface et augmentent ainsi le courant de fuite en surface, qui peut provoquer la combustion du matériau en plastique d'enrobage.

5.3.1.2 Distance d'isolement dans l'air (d_a)

Valeur minimale de la distance dans l'air, entre les bornes de polarité différente du dispositif isolé et l'embase.

NOTE Pour plus de détails, voir IEC 60664-1:2020, 4.6 et 5.1, qui présentent des exemples types de différentes formes de distances d'isolement.

5.3.1.3 Masse (m) du dispositif

Valeur maximale sans accessoires (matériels de montage).

5.3.1.4 Planéité du boîtier (embase) (e_c) (le cas échéant)

Écart maximal et minimal de planéité admissible pour l'embase et sa direction (convexe ou concave).

5.3.2 Inductance parasite (L_p)

Valeur maximale ou typique entre les bornes principales de chaque chemin de courant principal.

5.3.3 Capacités parasites (C_p)

Valeur maximale de la capacité parasite entre la ou les bornes principales spécifiées et la surface de refroidissement.

5.3.4 Tension d'apparition de décharge partielle (V_{iM} ou $V_{i(eff)}$) (le cas échéant)

Valeur de crête minimale, V_{iM}, ou valeur efficace, $V_{i(eff)}$, entre les bornes isolées et l'embase (pour les détails, voir IEC 60270:2015).

5.3.5 Tension d'extinction de décharge partielle (V_{eM} ou $V_{e(eff)}$) (le cas échéant)

Valeur de crête minimale, V_{eM}, ou valeur efficace, $V_{e(eff)}$, entre les bornes isolées et l'embase (pour les détails, voir IEC 60270:2015).

5.3.6 Résistances thermiques

5.3.6.1 Résistance thermique jonction – boîtier ($R_{th(j-c)X}$) pour les dispositifs spécifiés au niveau du boîtier

Valeur maximale de la résistance thermique de la jonction à un point de référence spécifié au niveau du boîtier (embase) par interrupteur "X" [par exemple de la diode (D), du thyristor (T), du transistor bipolaire à grille isolée (IGBT, Insulated-Gate Bipolar Transistor) (I) ou du MOSFET (M)].

5.3.6.2 Résistance thermique boîtier – dissipateur ($R_{th(c-s)}$) (le cas échéant)

Valeur maximale ou typique de la résistance thermique entre deux points spécifiés au niveau du boîtier et au niveau du dissipateur du dispositif spécifié au niveau du boîtier ("module"), lorsque le boîtier est monté conformément aux instructions de montage du fabricant.

5.3.6.3 Résistance thermique boîtier – dissipateur par interrupteur ($R_{th(c-s)X}$) (le cas échéant)

Valeur maximale ou typique de la résistance thermique entre les deux points spécifiés du boîtier et du dissipateur de l'interrupteur "X" [par exemple de la diode (D), du thyristor (T), de l'IGBT (I) ou du MOSFET (M)] des dispositifs isolés spécifiés au niveau du boîtier ("module"), lorsque le boîtier est monté conformément aux instructions de montage du fabricant.

5.3.6.4 Résistance thermique jonction – dissipateur ($R_{th(j-s)X}$) pour les dispositifs spécifiés avec dissipateur

Valeur maximale ou typique de la résistance thermique de la jonction à un point spécifié au niveau du dissipateur par interrupteur "X" [par exemple de la diode (D), du thyristor (T), de l'IGBT (I) ou du MOSFET (M)], lorsque le dispositif est monté conformément aux instructions de montage du fabricant.

5.3.6.5 Résistance thermique jonction – capteur ($R_{th(j-r)}$) (le cas échéant)

Valeur de la résistance thermique de la jonction à un capteur de température intégré, lorsque le dispositif est monté conformément aux instructions de montage du fabricant.

Il convient de présenter la position de cette résistance thermique dans le circuit équivalent de la résistance thermique.

5.3.7 Impédance thermique transitoire (Z_{th})

Impédance thermique en fonction du temps écoulé après une variation d'échelon de dissipation de puissance pour chaque résistance thermique spécifiée en 5.3.6 et qui doit être spécifiée selon une des manières suivantes.

6 Méthodes de mesure

6.1 Vérification de la valeur assignée de tension d'isolement

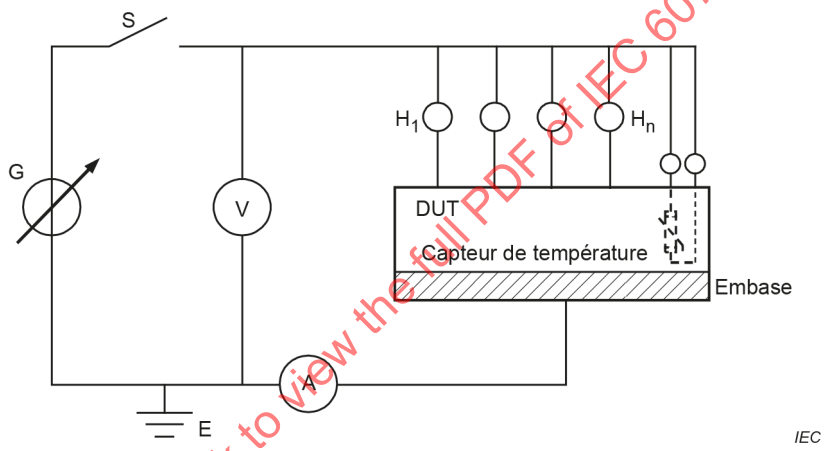
6.1.1 Vérification de la valeur assignée de tension d'isolement entre bornes et embase (V_{isol})

– Objectif

Démontrer la capacité du dispositif de puissance isolée à supporter la tension d'isolement assignée.

– Schéma du circuit

Voir Figure 1.



Légende

DUT	dispositif en essai
G	source de tension à haute impédance, capable de délivrer V_{isol}
S	interrupteur principal
V	voltmètre de mesure de V_{isol}
A	ampèremètre ou sonde de courant de mesure de Iisol
H_1...H_n	borne à potentiel élevé

Figure 1 – Schéma du circuit de base pour l'essai de tenue en tension au claquage de l'isolement ("essai à potentiel élevé") avec V_{isol}

La source de tension G est capable de délivrer la tension d'isolement, V_{isol}, alternative ou continue, avec une impédance interne élevée afin de limiter une éventuelle pointe de courant en cas de claquage du dispositif en essai (DUT, Device Under Test).

Toutes les bornes principales et les bornes de commande haute tension sont connectées ensemble, ainsi qu'à la borne de sortie à potentiel élevé H de la source de tension G. L'embase du DUT, c'est-à-dire sa surface de refroidissement métallisée et toutes les bornes basse tension sont connectées au potentiel de la masse E. Un ampèremètre ou une sonde de courant A est inséré pour mesurer le courant de fuite d'isolement.

Sous réserve d'un accord avec l'utilisateur, effectuer un essai d'isolement entre le capteur de température et les bornes (V_{Isol1}) (voir 6.1.2).

– Procédure d'essai

L'interrupteur S est fermé et la tension est augmentée progressivement jusqu'à la valeur spécifiée et maintenue à cette valeur pendant la durée spécifiée. Le courant mesuré sur l'ampèremètre A ne doit pas dépasser la valeur spécifiée. La tension est alors réduite à zéro.

– Conditions spécifiées:

spécifiées dans l'IEC 60664-1:2020:

- température ambiante ou du boîtier;
- V_{isol},;
- I_{isol} en tant que limite maximale d'essai;
- temps d'essai, t, si inférieur à 60 s.

6.1.2 Vérification de la valeur assignée de tension d'isolement entre le capteur de température et les bornes (V_{isol1})

– Objectif

Vérifier que la tension d'isolement entre le capteur de température et les autres bornes dans le cas où le capteur de température est connecté au potentiel de l'embase.

– Schéma du circuit

Voir Figure 2.

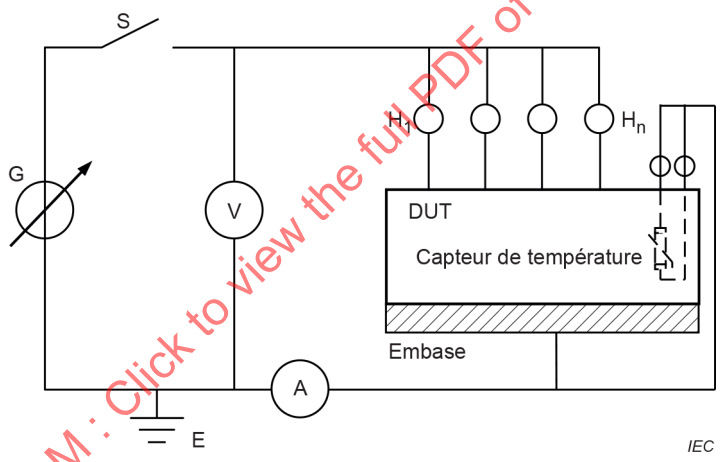


Figure 2 – Schéma du circuit de base pour l'essai de tension d'isolement entre le capteur de température et les bornes (V_{isol1})

– Description et exigences du circuit, procédure d'essai et conditions spécifiées

Similaire à celle décrite en 6.1.1, mais en option, une tension d'essai inférieure V_{isol1} peut être spécifiée et appliquée.

6.2 Méthodes de mesure

6.2.1 Tensions d'apparition et d'extinction de décharge partielle (V_i) (V_e)

Entre les bornes à potentiel élevé et l'embase (le cas échéant). Voir IEC 60270:2015 et IEC 60664-1:2020.

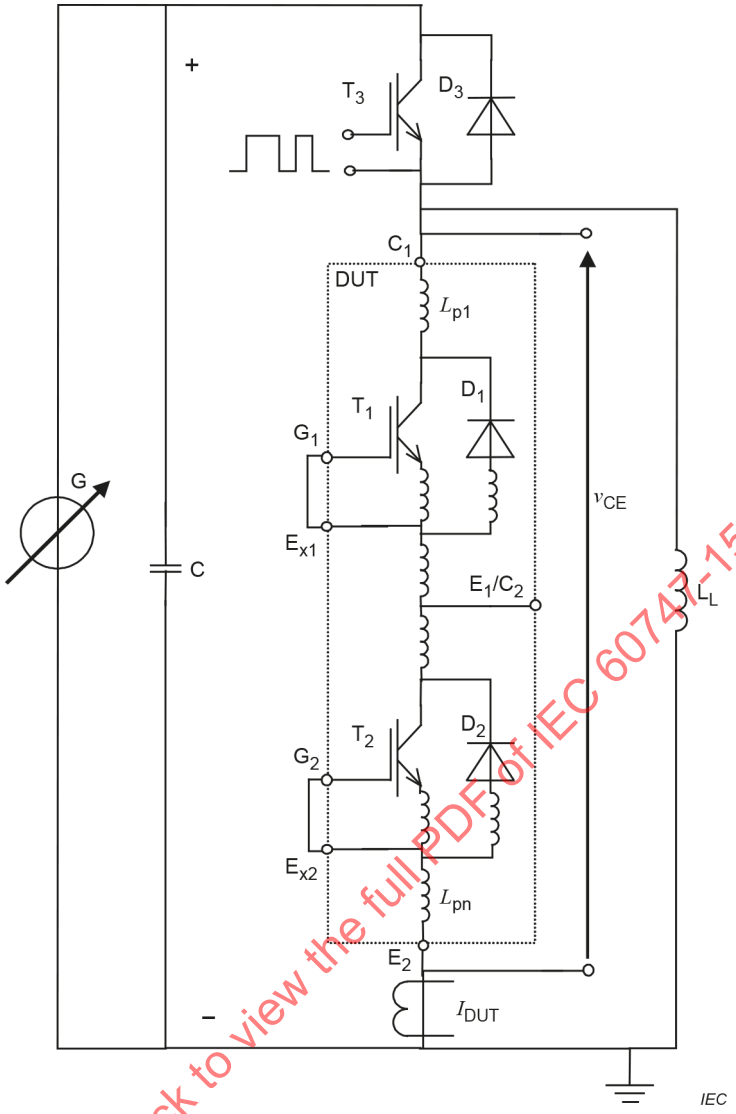
6.2.2 Inductance parasite (L_p)

– Objectif

Mesurer l'inductance parasite entre deux bornes principales.

– Schéma du circuit

Voir Figure 3.



Légende

DUT	dispositif en essai T_1+T_2, par exemple IGBT [simple ou double (représenté) ou branche d'une configuration triphasée], dispositif à MOSFET ou diode rapide
C	batterie de condensateurs principaux en tant que réservoir
L_L	inductance de charge, égale à au moins 100 fois l'inductance parasite
L_{p1} ...L_{pn}	parties de l'inductance parasite, L_p
I_{DUT}	sonde de courant
G	source de tension pour charger le condensateur
T_1	DUT, interrupteur supérieur (représenté comme IGBT à la Figure 3)
T_2	DUT, interrupteur inférieur (représenté comme IGBT à la Figure 3), facultatif
T_3	interrupteur IGBT auxiliaire

Figure 3 – Schéma du circuit pour la mesure des inductances parasites (L_p)

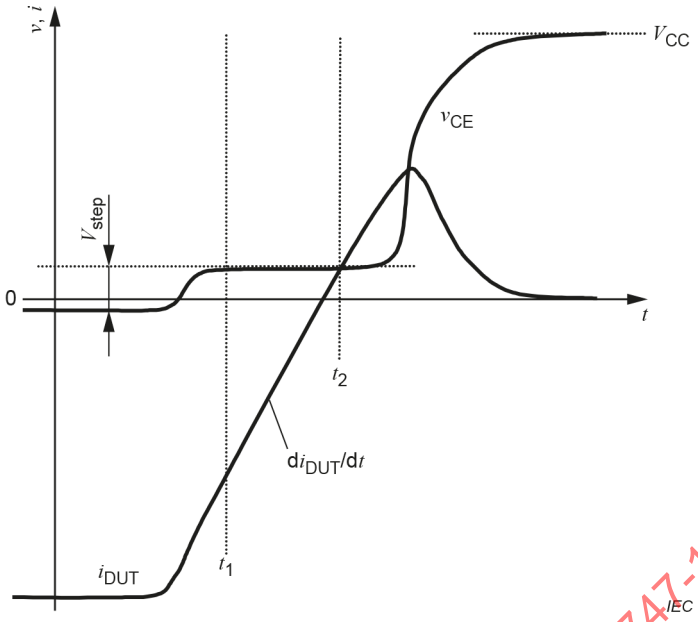


Figure 4 – Formes d'onde

– Description et exigences du circuit

Le circuit représenté à la Figure 3 est constitué d'une alimentation en courant continu G pour le réservoir de charge C, d'un interrupteur auxiliaire T_3, d'une unité de commande de grille T_3, du DUT inséré dans le montage d'essai avec les bornes de commande de grille court-circuitées, d'un oscilloscope à deux canaux qui mesure la tension v_{CE} entre les bornes principales "C_1" et "E_2", d'une sonde de courant qui mesure le courant i_{DUT} qui traverse la diode du DUT, connectée à l'oscilloscope à deux canaux. Cette méthode de mesure utilise une tension réduite, V_{CC}, et le di/dt des diodes incorporées dans le dispositif à la coupure, mesurant la tension aux bornes principales à l'extérieur. Cette méthode peut être utilisée pour les dispositifs à interrupteur simple, ainsi que pour les dispositifs à circuits en demi-pont (modules DOUBLES).

– Procédure de mesure

Les formes d'onde observées par cette mesure sont représentées à la Figure 4.

Une méthode à impulsions de courant est utilisée. Le transistor auxiliaire T_3 établit et coupe le courant de charge de la bobine d'inductance L_L. Lorsque T_3 se bloque, le courant circule en roue libre dans les diodes du DUT. Lorsque T_3 est à nouveau passant, il provoque la chute du courant dans les diodes suivant une pente presque linéaire di_{DUT}/dt. Pendant ce temps ($t_1 - t_2$), la tension aux bornes du DUT s'établit à l'échelon de tension, V_{step}, provoqué par l'inductance parasite interne lorsque le courant diminue (di_{DUT}/dt). La valeur de l'inductance parasite du chemin du courant principal peut être calculée à l'aide de l'équation suivante:

$$L_p = V_{step} / |(di_{DUT}/dt)| \quad (1)$$

Utiliser une barre omnibus de faible inductance (en feuilles) et une sonde de courant de faible inductance.

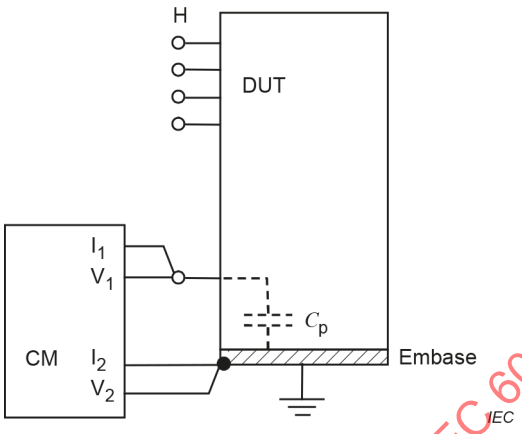
6.2.3 Capacité parasite borne – boîtier (C_p)

– Objectif

Mesurer la capacité parasite, C_p, entre la ou les bornes principales spécifiées et le boîtier (embase).

– Schéma du circuit

Voir Figure 5.



Légende

C_p capacité parasite

H borne à potentiel élevé

CM capacimètre

Figure 5 – Schéma de circuit pour la mesure de la capacité parasite (C_p)

– Procédure de mesure

Monter le dispositif sur un dissipateur relié à la masse conformément aux instructions de montage du fabricant. Raccorder le connecteur de la source de courant "I_1" du capacimètre CM à la borne spécifiée, et le connecteur "I_2" à la masse (embase) du DUT. Brancher le connecteur de mesure de tension du capacimètre aux points d'essai "V_1" et "V_2" à la masse. CM est réglé à la fréquence spécifiée. La capacité C_p peut être lue sur CM. Pour la mesure de la capacité de couplage totale, C_p, connecter toutes les bornes principales les unes aux autres et effectuer la mesure comme décrit ci-dessus.

– Conditions spécifiées:

- fréquence de mesure, f, du CM.

6.2.4 Caractéristiques thermiques

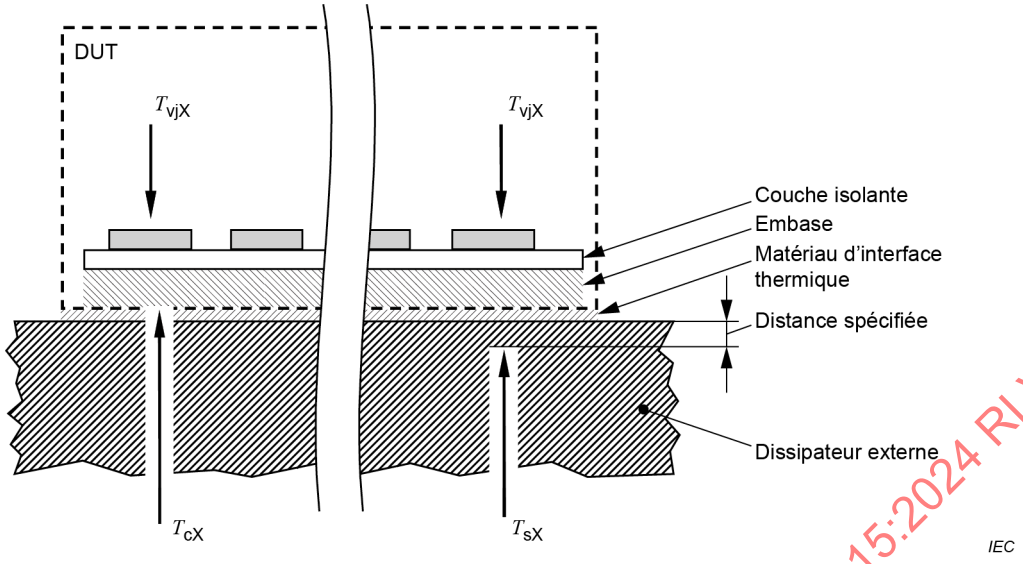
6.2.4.1 Description générale des méthodes de mesure

– Objectif

Mesurer les caractéristiques thermiques entre l'interrupteur et le système de refroidissement.

– Points de référence pour la mesure et la description de la température

Il convient d'employer les mêmes méthodes que pour le dispositif non isolé correspondant. La résistance thermique et l'impédance sont mesurées comme cela est décrit dans les documents suivants: l'IEC 60747-2:2016 pour les diodes, l'IEC 60747-6:2016 pour les thyristors, l'IEC 60747-7:2019 pour les transistors bipolaires, l'IEC 60747-8:2021 pour les FET et l'IEC 60747-9:2019 pour les IGBT.



Légende

T_{vjX} température de jonction de la puce X

T_{cX} température du boîtier sous la puce X

T_{sX} température du dissipateur sous la puce X

Figure 6 – Section transversale d'un dispositif de puissance isolé avec des points de référence pour la mesure des températures T_c et T_s

– Procédure de mesure

La vue en coupe d'un dispositif de puissance isolé est représentée à la Figure 6.

T_{cX} est mesurée au moyen d'un instrument de mesure de la température par le dessous, dans un petit trou qui traverse le dissipateur et tout matériau d'interface thermique sous l'interrupteur X (puce). T_{sX} est mesurée par le dessus au point le plus chaud accessible, au plus près de l'interrupteur X (puce), ou par le dessous dans un trou borgne spécifié dont le fond est à (2 ± 1) mm en dessous de la surface du dissipateur (à spécifier, montage d'essai type). T_{vjX} est déterminée à l'aide de méthodes indirectes décrites dans les documents individuels.

Les résistances thermiques, $R_{th(j\text{-}s)}$ et $R_{th(c\text{-}s)}$, dépendent de plusieurs paramètres mécaniques tels que le type et l'épaisseur du matériau d'interface thermique utilisé (il convient de la spécifier dans les instructions de montage du fabricant, par exemple 30 ∝m à 50 ∝m), l'écart maximal de planéité de la surface de refroidissement de l'embase du dispositif et du dissipateur et le couple de serrage des vis de fixation, selon des directives de montage spécifiées.

6.2.4.2 Jonction de résistance thermique au boîtier par interrupteur (X), $R_{th\ (j\text{-}c)X}$

$$R_{th(j\text{-}c)X} = (T_{vjX} - T_{cX})/P_X \quad (2)$$

où

X est D (diode), T (thyristor), I (IGBT), M (MOSFET), B (BJT);

T_{vjX} est la température de jonction virtuelle de l'interrupteur X;

T_{cX} est la température du boîtier (embase) sous l'interrupteur X (puce);

P_X est la dissipation de puissance à chaque interrupteur D, T, I, M et B.

Un deuxième indice peut être nécessaire pour distinguer plusieurs dispositifs dans un produit (par exemple les IGBT d'onduleurs et les IGBT de freinage).

6.2.4.3 Résistance thermique boîtier – dissipateur par interrupteur (X) $R_{th(c\text{-}s)X}$ ou par dispositif $R_{th(c\text{-}s)}$

$$R_{th(c\text{-}s)X} = (T_{cX} - T_{sX})/P_X \quad (3)$$

où

X est D (diode), T (thyristor), I (IGBT), M (MOSFET), B (BJT);

T_{cX} est la température mesurée au point spécifié du boîtier (comme ci-dessus) sous la puce;

T_{sX} est la température du dissipateur, mesurée au point de référence pour les essais T_s spécifiés;

P_X est la dissipation de puissance à chaque interrupteur D, T, I, M et B;

P est la dissipation de puissance appliquée du dispositif complet.

Un deuxième indice peut être nécessaire pour distinguer plusieurs dispositifs dans un produit (par exemple les IGBT d'onduleurs et les IGBT de freinage).

– Conditions spécifiées:
  - montage conformément aux instructions du fabricant;
  - conductivité thermique du matériau de l'interface thermique;
  - points de référence pour la mesure thermique.

NOTE L'Annexe B fournit une méthode de mesure de l'épaisseur d'un matériau d'interface thermique.

6.2.4.4 Résistance thermique jonction – dissipateur par interrupteur (X), $R_{th(j\text{-}s)X}$ (pour dispositifs spécifiés avec dissipateur)

$$R_{th(j\text{-}s)X} = (T_{vjX} - T_{sX})/P_X \quad (4)$$

où

X est D (diode), T (thyristor), I (IGBT), M (MOSFET), B (BJT);

T_{vjX} est la température de jonction virtuelle de l'interrupteur X;

T_{sX} est la température du dissipateur, mesurée au point de référence pour les essais T_s spécifiés;

P_X est la dissipation de puissance à chaque interrupteur D, T, I, M et B.

Un deuxième indice peut être nécessaire pour distinguer plusieurs dispositifs dans un produit (par exemple les IGBT d'onduleurs et les IGBT de freinage).

– Conditions spécifiées:
  - montage conformément aux instructions du fabricant;
  - conductivité thermique du matériau de l'interface thermique;
  - points de référence pour la mesure thermique.

6.2.4.5 Impédance thermique transitoire, Z_{th}

– Circuit et procédure de mesure

Ils sont fondés sur 6.2.4.2 à 6.2.4.4. Les documents individuels des dispositifs non isolés s'appliquent.

$$Z_{th(j\text{-}c)X} = (|T_{vjX}(0) - T_{cX}(0)| - |T_{vjX}(t) - T_{cX}(t)|) / P_X \quad (5)$$

$$Z_{th(c\text{-}s)X} = (|T_{cX}(0) - T_{sX}(0)| - |T_{cX}(t) - T_{sX}(t)|) / P_X \quad (6)$$

$$Z_{th(j\text{-}s)X} = (|T_{vjX}(0) - T_{sX}(0)| - |T_{vjX}(t) - T_{sX}(t)|) / P_X \quad (7)$$

– Conditions spécifiées:

- montage conformément aux instructions du fabricant;
- conductivité thermique du matériau de l'interface thermique;
- points de référence pour la mesure thermique.

7 Réception et fiabilité

7.1 Exigences générales

Outre les paragraphes suivants, les exigences applicables aux dispositifs non isolés indiqués dans les autres parties applicables de l'IEC 60747 s'appliquent.

7.2 Liste des essais d'endurance

Voir Tableau 1.

Tableau 1 – Essais d'endurance

Paragraphe	Essais d'environnement – désignation	Forme abrégée	Référence normative
7.2.1	Polarisation inverse à haute température ou blocage à haute température	HTRB	IEC 60749-5
7.2.2	Polarisation inverse à forte humidité et à haute température ou blocage à forte humidité et haute température	H^3TRB	IEC 60749-5
7.2.3	Aptitude aux cycles en puissance (charge)		IEC 60749-34
7.2.4	Stockage à haute température	HTS	IEC 60749-6
7.2.5	Stockage à basse température	LTS	IEC 60068-2-1
7.2.6	Cycles thermiques	TC	IEC 60749-25
7.2.7	Résistance à la température de brasage		IEC 60749-15
7.2.8	Brasabilité		IEC 60749-21
7.2.9	Chocs mécaniques		IEC 60749-10
7.2.10	Vibrations (fréquence variable)		IEC 60749-12

7.3 Critères de définition de la réception

Voir Tableau 2.

Tableau 2 – Caractéristiques définissant la réception pour les essais d'endurance et de fiabilité

Caractéristique définissant la réception	Critères d'acceptation	Conditions de mesure
I_{isol}	< USL	V_{isol} spécifiée
R_{th}	< USL	Instructions de montage
USL: limite supérieure de la spécification (Upper Specification Limit).		

7.4 Essais de type et essais individuels de série

7.4.1 Essais de type

Il convient de considérer l'expérience obtenue avec d'autres dispositifs de puissance à semiconducteurs isolés, utilisant des composants identiques ou similaires, tels que des interrupteurs ou des boîtiers, pour décider quels essais sont obligatoires.

Les essais de type sont effectués sur des produits neufs, par échantillonnage, afin de déterminer les valeurs assignées (valeurs limites) des caractéristiques électriques, thermiques, mécaniques et climatiques à faire figurer dans la fiche technique et d'établir les limites des essais pour de futurs essais individuels de série. Il convient que certains ou tous les essais soient répétés de temps en temps sur des échantillons prélevés de la production ou des livraisons courantes, afin de confirmer que la qualité du produit satisfait continuellement aux exigences.

Les essais de type à effectuer au minimum sont les suivants.

Il convient que les dispositifs de puissance à semiconducteurs isolés neufs soient soumis aux essais de type énumérés dans le Tableau 3, marqués par un "X" (X = obligatoire). Certains essais de type sont destructifs.

Tableau 3 – Essais minimaux de type et individuels de série pour les dispositifs de puissance à semiconducteurs isolés

Paragraphe	Points	Essais de type	Essais individuels de série	Destructif
5.2.1, 6.1	Tension d'isolement (V_{isol}), (V_{isol1})	X	X	
5.2.2, Annexe A	Courant de crête de non-rupture de boîtier	X [a]		X
5.3.1	Dimensions d'encombrement, ligne de fuite, distance d'isolement	X		
5.3.1.4	Planéité de l'embase	X	X [b]	
5.3.6, 6.2.4	Résistance thermique (R_{th})	X		
5.3.7, 6.2.4.5	Impédance thermique transitoire (Z_{th})	X		
5.3.2, 6.2.2	Inductance parasite (L_p)	X [a]		
5.3.3, 6.2.3	Capacité parasite (C_p)	X [a]		
5.3.4, 5.3.5, 6.2.1	Tension de décharges partielles (V_{iM} ou $V_{i(eff.)}$) / (V_{eM} ou $V_{e(eff.)}$)	X [a]	X [b]	

Paragraphe	Points	Essais de type	Essais individuels de série	Destructif
5.2.5.4	Force de traction sur les bornes (F_t)	X		X
7.2.6 [c]	Cycles thermiques	X		X
7.2.3 [c]	Cycles en puissance (charge)	X		X
7.2.9 [c], 7.2.10 [c]	Choc mécanique/vibrations	X		X
5.2.6	Caractéristiques climatiques	X [a]		

NOTE Il convient que les essais de tension d'isolement, de tension de décharge partielle, de ligne de fuite et de distance d'isolement soient basés sur chaque norme, et il convient que cette dernière soit appliquée à tout matériel final utilisant le dispositif de puissance à semiconducteurs isolé. Par exemple, voir IEC 62368-1, IEC 61287-1, etc.

[a] Essai de type uniquement pour les dispositifs avec valeurs maximales spécifiées.

[b] Essai individuel de série uniquement pour les dispositifs avec valeurs maximales ou minimales spécifiées.

[c] Voir le Tableau 1 pour les références normatives des essais.

7.4.2 Essais individuels de série

Il convient d'effectuer normalement les essais individuels de série sur 100 % de la production ou des livraisons courantes. Il convient de vérifier les valeurs assignées et les caractéristiques spécifiées dans les fiches techniques pour chaque critère ou éprouvette. L'essai individuel de série peut comprendre une sélection des dispositifs isolés dans les groupes d'essais individuels de série figurant dans le Tableau 3. Le Tableau 3 énumère les essais individuels de série à effectuer au minimum sur les dispositifs isolés. D'autres essais individuels de série sont effectués comme décrit dans les autres parties de l'IEC 60747 valables pour l'interrupteur donné.

Annexe A
(informative)

Méthode d'essai du courant de crête de non-rupture de boîtier [1]

A.1 Objectif

Prouver la capacité du dispositif de puissance isolé contenant des transistors bipolaires, des IGBT ou des MOSFET utilisés comme interrupteurs à supporter le courant de crête de non-rupture de boîtier assigné, sans provoquer de rupture ("explosion") du boîtier ni le dégagement d'un jet de plasma ou de rejet de particules massives. Il s'agit d'un essai destructif.

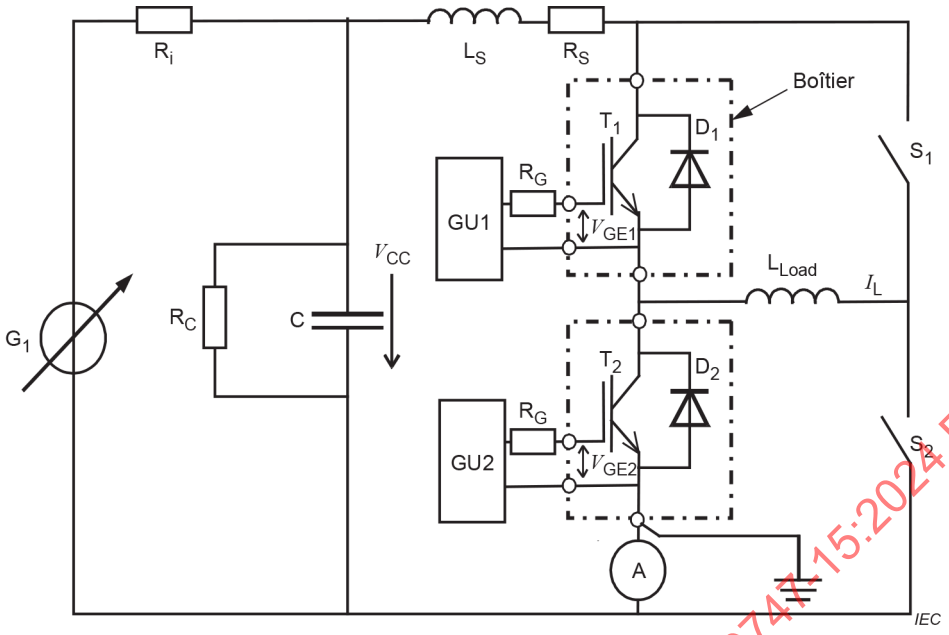
Une rupture de boîtier est provoquée par un arc intérieur ou une pression de vapeur, lorsque l'énergie ou le courant délivré par une source extérieure dépasse la limite spécifiée. L'arc ou la pression de vapeur est induit dans un boîtier (encapsulation) de dispositifs de puissance défaillants en étant alimenté par l'énergie ou le courant stocké d'une source de puissance extérieure. Il convient que le courant ou l'énergie critique pour les boîtiers après la défaillance du dispositif soit déclaré comme un élément des propriétés environnementales du boîtier. De plus, il convient d'éviter toute explosion accidentelle pour le semiconducteur, ainsi que les autres parties électriques.

NOTE L'Annexe A est applicable sous réserve d'un accord avec l'utilisateur.

A.2 Schéma du circuit

Voir Figure A.1.

[1] Encore en délibération.



Légende

A	ampèremètre pour mesurer le courant du dispositif, qui peut être le courant de crête de non-rupture de boîtier, si le boîtier n'a pas éclaté, surveillé par une sonde de courant ayant une faible inductance
C	batterie de condensateurs de ligne, pouvant être chargée à la tension maximale
D_1	diode antiparallèle de T_1, côté haut
D_2	diode antiparallèle de T_2, côté bas
G_1	source de tension d'alimentation en courant continu, V_{CC}, qui peut être déconnectée du réseau dans toutes les conditions
GU_1	unité de commande de grille de T_1
GU_2	unité de commande de grille de T_2
L_{Load}	inductance de charge
L_s	inductance parasite du circuit (valeur spécifiée)
R_c	résistance de décharge à des fins de protection
R_{G1}	résistance de grille de T_1
R_{G2}	résistance de grille de T_2
R_i	résistance interne de la source
R_s	résistance fusible, le plus souvent nulle
S_1	interrupteur auxiliaire (IGBT), côté haut
S_2	interrupteur auxiliaire (IGBT), côté bas
T_1	interrupteur IGBT côté haut = dispositif en essai (DUT)
T_2	interrupteur IGBT côté bas
I_L	courant de charge
V_{GE1}	tension de grille de T_1
V_{GE2}	tension de grille de T_2

Figure A.1 – Schéma du circuit pour l'essai du courant de crête de non-rupture de boîtier